컴퓨터를 이용한 순차 논리 회로의 설계 (동기식 순차 논리 회로의 경우)

論 文
33~4~2

Computer Aided Design of Sequential Logic Circuits (Case of Synchronous Sequential Logic Circuits)

金 敬 植*·趙 東 燮**·黃 熙 隆***
(Kyung-Sik Kim · Dong-Sub Cho · Hee-Yeung Hwang)

요 약

본 논문은 마스크 방식 (MASK Method)을 이용해서 동기식 순차 논리 회로(Synchronous Sequential Logic Circuit)를 계산기로 설계할 수 있도록 하는 프로그램을 제시한다.

이 프로그램은 입력으로 이미 상태의 수가 최소화되고 상태 지정이 완료된 상태 천이표 (State Transition Table)를 받아 JK, T, D와 RS의 네 가지 플립플럽(Flip-Flop)에 대해 각각 최저 비용의 회로를 구성해 보고, 설계 비용이 적게 드는 기억 요소와 그것을 사용한 회로의 연결 방법을 선택하여 출력으로 낸다.

Abstract

This paper presents the computer program to design the synchronous sequential logic circuit. The computer program uses the MASK method to get the circuit of optimal cost.

The computer program takes as an input, the minimal reduced state transition table where each state has its internal code. As an output, the optimal design of synchronous sequential logic circuit is generated for each flipflop type of JK, T, D, and RS respectively. And these circuits for 4 flipflop types are evaluated and sorted in ascending order of their costs, so that the user can select the proper flipflop type and its circuit.

Furthermore, the proposed computer program may be applied to state assignment with its facility of cost evaluation.

1. Introduction

In our daily activites, the uses of various synchronous sequential circuits are encountered. The elevator control systems, the traffic light control systems in the roads, and train and subway control systems, are examples of synchronous sequential logic circuits in action.

The synthesis procedure of synchronous sequential logic circuit is shown in Fig. 1.[6] But these steps have a lot of decision factors and selection factors, and they are so complex that design automation would be needed.

At the moment, automated logic synthesis is still in a rudimentary phase of development. In the last few years an increasing number of investigations have been performed. But general approach to logic synthesis is still missing.[12)-16)]

In this paper, the proposed method follows the general approach to get the circuit of optimal design cost. It takes as an input, the state transition table that is minimal reduced with each state having its internal code, and outputs switching functions of synchronous sequential logic circuits for 4 flipflop types of JK, T, D, and RS. The block with dotted

*正 會 員 : 서울大 工大 電子計算機工學科 博士課程
**正 會 員 : 서울大 工大 電子計算機工學科 博士課程
***正 會 員 : 서울大 工大 電子計算機工學科 教授
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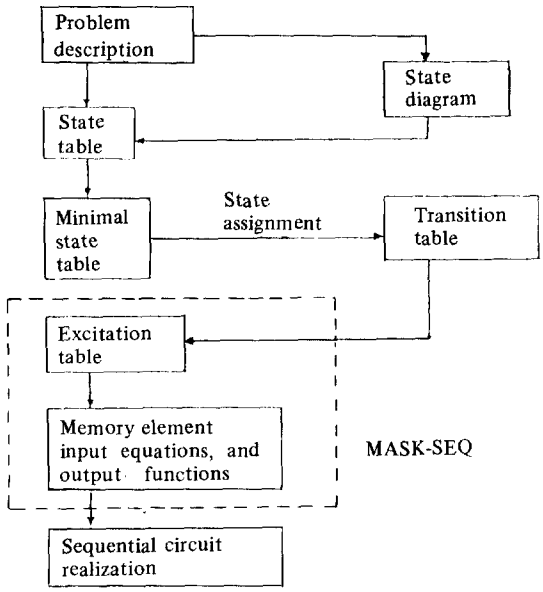

Fig. 1. Synthesis process.

line in Fig. 1 shows the parts automated in this paper, and is named "MASK-SEQ".

Furthermore, the proposed computer program may be expanded to state assignment and up to state minimization.

2. Analysis of Synchronous Sequential Logic Circuit for Design Automation

The synchronous sequential logic circuit is composed of two parts: the combinational logic circuits and the memory devices, flipflops. The number of flipflops is determined by the number of state variables. Thus it is the combinational logic circuit that can be reduced when state variables are fixed.[4),5)]

How to assign the internal code to each state, is critical in reduction of the combinational part. Even after state assignment, the reduction of the combinational part depends on how to determine the switching functions i.e., the next state functions, and output functions.[8)-10)]

While the problem state assign unsolved, the reduction of the combinational part after state assignment is accomplished in this paper by using the MASK method already developed into multiple-output-switching-functions.[1)-3)]

The design procedure in this paper follows the general steps of Fig. 1, but differs from the traditional methods in the way of getting the next state functions and output functions.[6),7),11)] This paper uses multiple output switching functions developed from the MASK method while the traditional one uses single output switching function for each flipflop input.[1)-3)]

This multiple output switching function is represented in the form of "sum of product", applicable to PLA directly. The more products are shared, the lower is the design cost.

3. Procedure for the MASK-SEQ

The flowchart of MASK-SEQ is shown in Figure 2. The followings are the steps for MASK-SEQ;

Step 1: Read the present state Q, inputs X, next states QNEXT, and output Y from the state transition table.

Step 2: Obtain the excitation table, at first, for JK flipflop type, in the next sequences of T, D, and RS flipflop types, by the algorithm provided in 3-1.

Step 3: Perform the multiple output switching functions with the inputs of Q, X and the right side of excitation table. (Get the Irredundant Paramount Prime Implicants using the MASK method)

Step 4: Validity check. Test if the result of step 3 is correct by the algorithm provided in 3-2.

Step 5: If the result is not valid, print error messages and go to step 7.

Step 6: Evaluate the cost of the valid result of step 3, by the algorithm provided in 3-3.

Step 7: If all the flipflop types are not tested, go to step 2.

Step 8: Sort the results of cost evaluations in step 6, for 4 types of flipflop in ascending order of the number of produces, the number of gates, and the number of connection lines.

Step 9: Stop.

Program "MASK-SEQ" is written in the language of FORTRAN.

3 -1 Algorithm for the Generation of the Excitation Table

Table 1 shows the excitation maps for 4 flip-flop types where Q stands for present state, QNEXT for next state. Unused state is also handled with QNEXT having don't care, X.

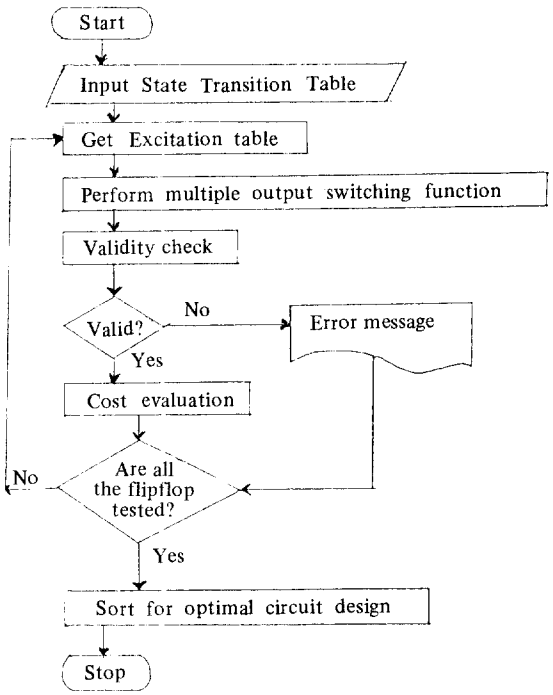

Fig. 2. Flowchart of MASK-SEQ.

1) JK flipflop

```
if QNEXT = X then J = X ; K = X ; return
endif
if Q = 0
   then J = QNEXT ; K = X
   else J = X ; K = QNEXT
endif
```

2) T flipflop

```
if QNEXT = X then T = X ; return endif
if Q + QNEXT = 1
   then T = 1
   else T = 0
endif
```

3) D flipflop

```
D = QNEXT
```

4) RS flipflop

```
if QNEXT = X then R = X ; S = X ; return
endif
if Q = 0
   then if QNEXT = 0
          then S = 0 ; R = X
          else S = 1 ; R = 0
        end if
   else if QNEXT = 0
          then S = 0 ; R = 1
          else S = X ; R = 0
        endif
endif
```

Table 1. Excitation maps for 4 flipflops

Q	QNEXT	J K	T	D	R S
0	0	0 X	0	0	X 0
0	1	1 X	1	1	0 1
1	0	X 1	1	0	1 0
1	1	X 0	0	1	0 X
0	X	X X	X	X	X X
1	X	X X	X	X	X X

(unused state)

3-2 Algorithm for Validity Check

Validity check is performed by comparing the next states and outputs derived from the result, with those of the state transition table.

Step 1: Get one entry of Q table.

Step 2: Choose the rows of the RESULT table that covers the given input in step 1. Set the next state function.

Step 3: Get next states according to table 2.

Step 4: Compare the next states and output with corresponding QNEXT table entry.

Step 5: If they are not same, then go to step 7, else go to step 1.

Step 6: Print success meassage; return

Step 7: Print error message: return

3-3 Algorithm for Cost Evaluation

The output of the program presented in this paper is RESULT table. It is based on "sum of

Table 2. State transition

J K	QNEXT	T	QNEXT	D	QNEXT	S R	QNEXT
0 0	Q	0	Q	0	0	0 0	Q
0 1	0	1	Q′	1	1	0 1	0
1 0	1					1 0	1
1 1	Q′					1 1	invalid

product" representation, especially adequate to Programmable Logic Array (PLA).

Consequently, the number of terms which means product in "sum of product" is the first factor that minimize the size of PLA. Second factor is the number of gates (AND gates or OR gates), and third factor is the number of connection lines. Cost evaluation is to determine these three factors.

Step 1: Count the rows of RESULT table. It is the number of terms.

Step 2: Count the number of AND states in the field if INPUT VARIABLE of RESULT table.

Step 3: Count the number of OR gates in the field of COMMONALITY FOR SELECTED PARAMOUNT PI of RESULT table.

Step 4: Count the number of connection lines that are the lines between inputs, present states and AND gates, the lines between AND states and OR gates, the lines between OR gates and flipflop input pins.

4. Example of MASK-SEQ and Comparison to Traditional Method

The table 3 is the state transition table for modulo-5 up counter.

Table 3. State tansition table for Modulo-5 up counter

Q(1:3)			QNEXT(1:3)		
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

The FORTRAN version of the MASK-SEQ was run on CROMEMCO SYSTEM THREE. Using this table as an input data, the MASK-SEQ produces the followings;

OPTIMAL FLIP/FLOP ORDER

ORDER	FLIP/FLOP	# TERM	#GATE	#CONNECTION
1	T	4	2	7
2	JK	4	2	10
3	RS	4	4	14
4	D	4	5	13

****** T FLIP/FLOP *****

: INPUT VARIABLES :			COMMNALITY FOR SELECTED PARAMOUNT PI		
: A	B	C :	F1	F2	F3
: 1	X	X :	1	0	0
: 0	X	X :	0	0	1
: X	1	1 :	1	0	0
: X	X	1 :	0	1	0

Here, # TERM, #GATE, and #CONNECTION mean the total number of terms, the total number of gates, and the total number of connection lines, respectively. The sorted result shows that T flipflop is optimal.

And A, B, C mean the memory elements, flipflops, and F1, F2, F3 mean TA, TB, TC respectively. The computer output above is interpreted as follows,

$TA = A + BC$; $TB = C$; $TC = A'$

The circuit for this result is shown in Fig. 3.

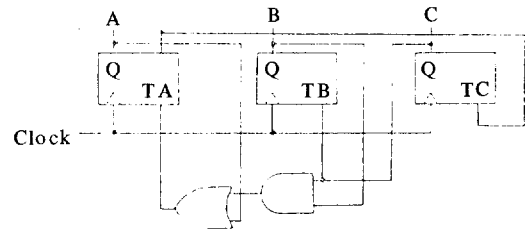

Fig. 3. Logic diagram of a Modulo-5 up counter

In the traditional method, the excitation table is made from Table 3, and is shown in Table 4. Next, for each flipflop input, switching function is obtained. In Fig. 4, Karnaugh Map Method is used to get it.[8)-10)]

Table 4. Excitation table of Modulo-5 up counter

A	B	C	A′	B′	C′	TA	TB	TC
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X

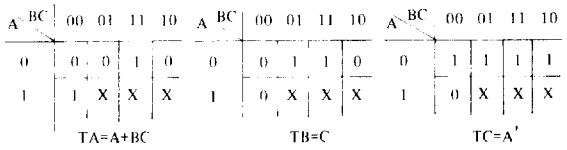

Fig. 4. Each single switching function using Karnaugh Map.

The result is same as that of MASK-SEQ. But there is a difference between MASK-SEQ and the traditional method. The former uses multiple output switching function while the latter uses single output switching function. It is certain that the result of multiple output switching function will be lower in cost than the result of single ones.

5. Expansion to State Assignment

Future direction of this study is toward state assignment. In that case, input is minimal reduced state table that has state in symbol, not internal coded.

There should be a policy to assign the internal code to each state, so that finite state assignments can be tested.[8)-10)] Assuming such a policy is determined, there are finite state transition tables.

For each state transition table, run MASK-SEQ. Then save the results and cost evaluation. By choosing lowest cost for each flipflop type, the best state assignment for that flipflop is determined, and its circuit is obtained.

6. Conclusions

In order to synthesize the synchronous sequential logic circuits from the state transition table, this paper presents a computer program which produces the circuit of optimal cost. Optimality here means minimization of the number of terms, of the number of gates, of the number of the connection lines.

The number of fan-in or fan-out of gate is not considered in constructing the circuit because the usage of PLA frees the users from fan-in or fan-out, but optimality leads to the design with less fan-in.

Finally, the advantages and features of the presented computer program are concluded as follows;

(1) From the state transition table, an optimal circuit for each of 4 flipflop types (JK, T, D, RS) is obtained.

(2) Use of the MASK method developed into the multiple output switching function in finding the optimal circuit.

(3) The state assignment problem can be appropached toward solution by trying the finite number of the transition tables that can be possibly derived from the minimal state table.

(4) Computer aided design enables us to obtain the fast and correct design.

(5) The FORTRAN version of this program can handle the state transition table of 32 states. But larger state transition table can be handled by changing some parts of the program.

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