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Acquisition Behavior of a Class of Digital Phase-Locked Loops

(Digital Phase-Locked Loops의 위상 포착 과정에 관한 硏究)

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(C. K. An and C. K. Un)

要 約

본 논문에서는 Reddy와 Gupta가 제안한 1차 및 2차 디지탈 phase-locked loops(DPLL)에 관하여, 잡음이 없는 상태에서 위상 포착 과정을 연구하여 새로운 결과를 얻었다. 먼저 양자화 단계 L과 위상 오차 상태수 N이 위상 포착 과정에서 중요한 위치를 차지하는 것을 보였다. 고정된 L단계 양자화 장치에서, N이 증가함에 따라, 포착 시간은 증가하고 동기 구속 범위는 감소하는 반면, 정상 상태에서의 위상 오차편차는 감소한다. L이 증가하는 경우에는, 포착 시간은 감소하고 동기 구속 범위가 증가하며, 또한 정상 상태에서의 위상 오차는 L의 변화에 거의 영향을 받지 않는다. 포착 과정에서 루프 필터가 미치는 영향에 관해서도 연구되었다. 필터의 변수를 크게 할수록 포착 시간을 줄이며, 구속 범위를 증가시킬 수 있다. 그러나 이 경우 정상 상태에서의 위상 오차 편차는 증가된다. 분석 결과들은 컴퓨터 시뮬레이션에 의해 입증했다.

Abstract

In this paper new results relating to the acquisition behavior of a class of first- and second-order digital phase-locked loops (DPLL) originally proposed by Reddy and Gupta are presented in the absence of noise. It has been found that the number of quantization levels L and the number of phase error states N play important roles in acquisition. For a given L-level quantizer, as N increases, the acquisition time increases, and the lock range decreases. However, the deviation of the steady state phase error decreases in this case. When L increases, the acquisition time decreases, and the lock range increases. However, variation of L affects little for the steady state phase error. In addition, the effects of a loop filter on acquisition have also been considered. One can get smaller acquisition time and larger lock range as the filter parameter value becomes larger. However, deviation of the steady state phase error increases in that case. Analytical results have been verified by computer simulation.

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I. Introduction

In recent years, as a result of the rapid advances of large scale integrated (LSI) digital circuits and digital computers, many subsystems including phase-locked loops are becoming

digitalized, and this trend will continue. Digital systems have in general the advantages of reduced size and cost, and increased reliability and stability compared with their analog counterparts. Therefore, the use of a digital phase-locked loop (DPLL) can avoid the problems that are encountered in an analog phase-locked loop (APLL), such as voltage controlled oscillator (VCO) drift, phase detector inaccuracy, and loop filter saturation problems. However, some inherent disadvantages of digital circuitry, that is, quantization and round off error, and overflow problem, exist also in DPLL. Nevertheless, considering the advantages of the DPLL, these disadvantages are not serious problems.

Although APLL has been studied extensively in the past twenty years, little analytical study on DPLL's has been done despite of its increasingly widespread usage. Accordingly, the general acquisition behavior of a DPLL is not well understood.

Several different forms of DPLL have so far been proposed. A DPLL system was proposed and studied by Gill and Gupta[1], and later by Reddy and Gupta[2]. Additional work was done by Weinberg and Liu[3]. Another DPLL system with a square-wave input was analyzed by Cessna and Levy[4], and later by Yamamoto and Mori[5]. Random-walk sequential loop filters were used in their system. The transient and steady state analyses were performed by Cessna and Levy, assuming that the input signal was corrupted by additive white Gaussian noise.

Another DPLL was studied by Pasternack and Whalin[6]. This DPLL runs with a high degree of stability. Tracking of the Holmes' loop[7] is accomplished by sampling the input waveform at zero crossings, accumulating these samples, and incrementing the phase of clock in such a direction as to bring the accumulated value toward zero. Recently, Lindsey and Chie studied acquisition behavior of a first order DPLL[8].

In this paper, using the DPLL model originally proposed by Reddy and Gupta[2], the acquisition behaviors of the first and second order DPLL in the absence of noise are studied. Specifically, we are interested in the general acquisition behavior, the acquisition time, the lock range, and the effects of quantization on acquisition. One may note that Reddy and Gupta's DPLL is the most analogous to the conventional sinusoidal APLL. This is the reason why we have chosen their DPLL for our study.

Following this introduction, in section II we briefly describe the DPLL system under study. In section III, discrete time analyses of the first- and second-order DPLL's including the phase error behavior on the phase plane are carried out. In section IV, analysis on acquisition time of the DPLL's is done, and the results will be verified by computer simulation. In addition, lock range of the DPLL's will be considered in section V. Finally, conclusions will be made in section VI.

II. Description of DPLL and its Operation

A block diagram of the DPLL under study is shown in Fig. 1. It consists of a sampler, a quantizer, a digital loop filter, and a digital clock with a local oscillator. A model of the DPLL system is depicted in Fig. 2. The loop filter used for the second order DPLL is shown in Fig. 3. Comparing the DPLL with a conventional APLL, the sampler corresponds to a phase detector in APLL, and the digital clock corresponds to a VCO. It differs markedly from the APLL in both structure and mechanism of locking.

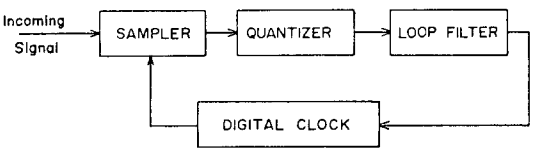

Fig. 1. Block diagram of DPLL.

The operation of the DPLL is as follows. At $t = t(0)$ the digital clock generates a signal for the sampler so that the sampler takes from an

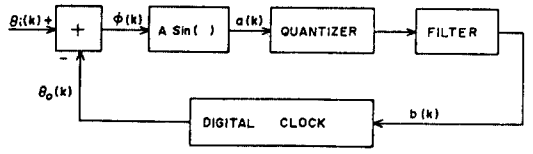

Fig. 2. Model of DPLL.

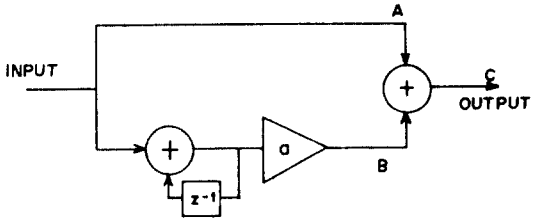

Fig. 3. DPLL loop filter.

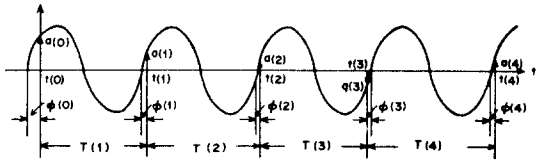

Fig. 4. Input signal waveform and sampled values by DPLL.

incoming sinusoidal signal a sample with the magnitude of a(0) as shown in Fig. 4. It is quantized by an L-level uniform quantizer without dead zone, and then the output of the quantizer is filtered by a digital loop filter. The digital filter output, b(0), is a correction command to the digital clock. The clock generates a sampling signal after the digital clock counts (N-b(0)) pulses from the local oscillator, where N is an integer representing the number of states that the phase error can take in modulo 2π. In this case the next sampling time period is $T(1) = T - (T/N)\,b(0)$ where $T = 2\pi/\omega_o$ (ω_o is the carrier frequency of the incoming signal). Due to a new sampling signal at $t = t(1)$, the sampler takes another sample with the magnitude of $a(1) = \sin\phi(1)$. The phase error between the positive going zero crossing point of the incoming signal and the phase of the sampling signal from the clock is $\phi(1)$ at $t = t(1)$. This process continues. The second sampling point at t=t(1) is nearer to the positive going zero crossing than the first sampling point at t=t(0), thus reducing the phase error. The third sample is taken after T(2) [=T-(T/N) b (1)] seconds, moving the sampling point still closer to the positive going zero crossings. The fluctuating range of the phase error lies within $\pm 2\pi/N$ with the average phase error and the magnitude of minimum error lying within π/N. Since the DPLL is an all digital feedback system, no perfect locking is possible. However, the oscillating range of the steady state phase error can be kept within some allowable range for a specific application. Details of the DPLL system may be found in reference[2].

III. Mathematical Model of DPLL

To obtain the equations of DPLL operation, let the incoming analog signal with the amplitude A and phase angle $\theta_i(t)$ be

$$s(t) = A \sin(\omega_o t + \theta_i(t)). \qquad (1)$$

Then, the output of the digital loop filter, b(k), may be expressed as

$$b(k) = D[Q[A \sin\phi(k)]] \qquad (2)$$

where Q(•) is the quantized value, D(•) indicates the filtering operation by the digital loop filter, $\phi(k) = \theta_i(k) - \theta_o(k)$, and $\theta_o(k)$ is the output phase sample at the k_{th} instant. The sampler takes a sample of the incoming signal when an impulse is sent by the digital clock. This discrete timing information constitutes the output phase of the clock. On each sampling instant the clock phase advances by 2π radians since each sampling period corresponds to one full cycle as far as the digital clock is concerned. As shown in Fig. 3, the digital low-pass filter used in our second-order DPLL system is a proportionality plus accumulator, whose transfer function corresponding to 1+a/s in the analog domain is

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* This section is largely based on the work of Ready and Gupta[2], but is presented in slightly different form.

$$D(z) = (1+a)\frac{z - \frac{1}{1+a}}{z-1}, \qquad (3)$$

where "a" is a constant.

Note from Fig. 4 that

$$t(k) = \sum_{j=1}^{k} T(j) + t(0) \qquad (4)$$

where

$$T(k) = T - \frac{T}{N} b(k-1). \qquad (5)$$

Hence, the total output phase up to k is

$$\Phi_o(k) = \sum_{j=1}^{k} \omega(j)T(j) = 2\pi k \qquad (6)$$

where $\omega(k)$ [$=2\pi/T(k)$] is the instantaneous frequency in radians per second in the k_{th} clock period. This $\Phi_o(k)$ may be expressed in terms of the frequency ω_o of the incoming signal as

$$\Phi_o(k) = \omega_o t(k) + \theta_o(k). \qquad (7)$$

Hence, from (4), (5) and (7) we have

$$\theta_o(k) = \sum_{j=1}^{k} (\omega(j) - \omega_o) T(j) - \omega_o t(0). \qquad (8)$$

Introducing D(z) for the loop filter transfer function in z-domain and using (5) and (8), we obtain the output phase as

$$\theta_o(k) = \sum_{j=1}^{k} \omega_o \frac{T}{N} D(z)\, Q[A \sin\phi(j-1)] - \omega_o t(0), \qquad (9)$$

from which we have a difference equation for the output phase

$$\theta_o(k+1) = \theta_o(k) + \omega_o \frac{T}{N} D(z)\, Q[A \sin\phi(k)]. \qquad (10)$$

Since $\Phi(k) = \theta_i(k) - \theta_o(k)$, (10) may be re-written as

$$\phi(k+1) - \phi(k) + \omega_o T/N\ D(z)\ Q[A \sin\phi(k)] = \theta_i(k+1) - \theta_i(k). \qquad (11)$$

Also, we obtain from (2), (4), (5) and (8) the total time up to k_{th} sampling:

$$t(k) = t(0) + k\ T - \frac{\theta_o(k) + \omega_o t(0)}{\omega_o} \qquad (12)$$

Letting $t(0) = 0$ and $\theta_o(0) = 0$ for simplicity of analysis, we have

$$t(k) = k\,T - \frac{\theta_o(k)}{\omega_o} \qquad (13)$$

Eqs. (10), (11) and (13) are important for our subsequent analyses of the DPLL system. Using these equations, one can plot the responses of the first (a = 0) and second-order DPLL to the phase step input of θ. Figs. 5 and 6 show these plots with one-level (L = 1) and three-level (L=3) quantizers, respectively.

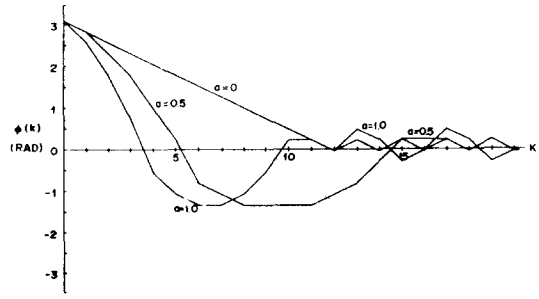

Fig. 5. Response to phase step input of first- and second-order DPLL with one-level quantizer [N = 24, L = 1, $\theta_i(0)$ = 3.1 rad].

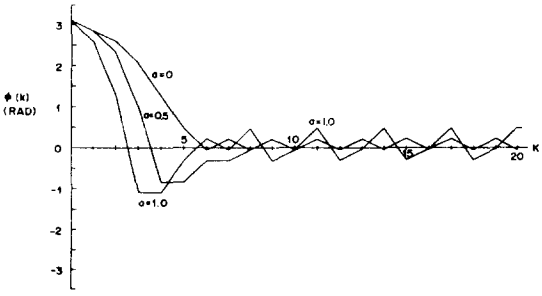

Fig. 6. Response to phase-step input of first- and second-order DPLL with three-level quantizer [N = 24, L = 3, $\theta_i(0)$ = 3.1 rad].

If the input is a sinusoidal signal with the frequency step input of ω, the input phase at the k_{th} sampling instant is given by

$$\theta_i(k) = (\omega - \omega_o)\, t(k). \tag{14}$$

Hence, with aid of (13) we have

$$\theta_i(k) = \frac{\omega - \omega_o}{\omega_o}(2\pi k - \theta_o(k)). \tag{15}$$

Thus,

$$\theta_i(k+1) - \theta_i(k) = \frac{\omega - \omega_o}{\omega_o}[2\pi - \omega_o \cdot \frac{T}{N} D(z)\, Q\,[A \sin\phi(k)]] \tag{16}$$

Consequently, substituting (16) into (11), we obtain the equation for phase error

$$\phi(k+1) = \phi(k) - \omega \frac{T}{N} D(z)\, Q\,[A \sin\phi(k)] + \left(\frac{\omega - \omega_o}{\omega_o}\right) 2\pi. \tag{17}$$

Using the above equation, one can plot the frequency acquisition processes of the first-and second-order DPLL with different parameter values. These are shown in Figs. 5.7 through 9.

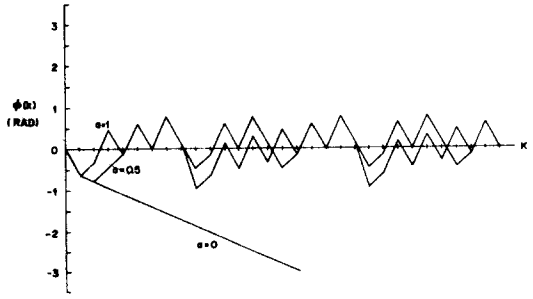

Fig. 7. Responses to frequency step input of first- and second-order DPLL with one-level quantizer [N = 24, L = 1, $\omega/\omega_0 = 0.9$].

In these figures, it is seen that as the number of quantizer levels L increases and/or as the number of phase error states N decreases, the lock range becomes large. Also, as N increases, deviation (i. e., maximum amplitude of phase

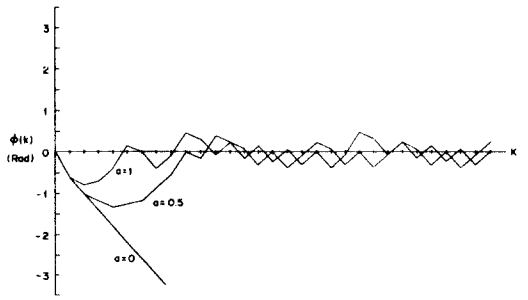

Fig. 8. Responses to frequency step input of first- and second-order DPLL with one-level quantizer [N = 12, L = 1, $\omega/\omega_0 = 0.9$].

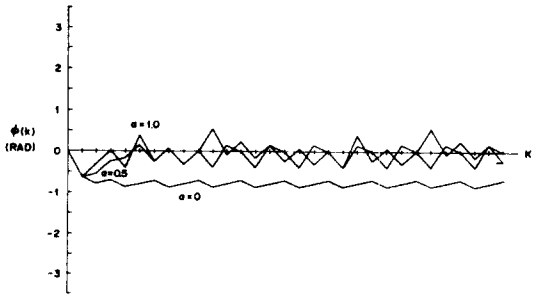

Fig. 9. Responses to frequency step input of first- and second-order DPLL with three-level quantizer [N = 24, L = 3, $\omega/\omega_0 = 0.9$].

error oscillation) of the steady state phase error decreases, but acquisition time increases. For a given N, as the number of quantizer levels and the filter parameter value 'a' increases, acquisition time decreases. Also, as the value of the filter parameter 'a' increases, deviation of the steady state phase error increases.

In addition, one can draw phase plane plots showing the phase change (i.e., $\Delta\phi_k = \phi(k+1) - \phi(k)$) as a function of $\phi(k)$. Phase plane plots of the first- and second-order DPP's with different parameter values are shown in Figs. 10 through 14. One can note that, unlike in APLL in which the points of the phase error on the phase plane gradually reach the origin, the points of the DPLL phase error in the steady state oscillate between two points or more.

To obtain acquisition time, one must find the required number of steps for a DPLL to achieve the steady (locking) state. Note that for a frequency step input of ω, the phase error is

$$\phi(k) = \omega t(k) - 2\pi k. \tag{18}$$

Hence, the required number of steps for acquisition is

$$k = \frac{\omega t(k) - \phi_{ss}}{2\pi}, \tag{19}$$

where ϕ_{ss} is $\phi(k)$ of (18) in the steady state. Substituting (13) and (9) into (19), we can obtain the following explicitly in terms of DPLL parameters;

$$k = \frac{1}{2\pi}\left[\omega\left[kT - \frac{T}{N}D(z)\sum_{j=o}^{k-1} Q[A\sin\phi(j)]\right] - \phi_{ss}\right]. \tag{20}$$

Henceforth we assume for simplicity that amplitude of the sinusoidal input is unity (i.e., A=1), and the initial condition $\phi(0)$ is zero. We now discuss (20) specifically for the first- and second-order loop with a one or multi-level quantizer.

1. First-Order Loop with One-Level Quantizer

For a first-order DPLL, we have D(z) = 1. Note that before the DPLL is in lock condition, we have

$$Q[\sin\phi(j)] = -1 \quad \text{for } \omega < \omega_o$$

and

$$Q[\sin\phi(j)] = 1 \quad \text{for } \omega > \omega_o$$

Thus, we replace $\sum_{j=0}^{k-1} Q[\sin\phi(j)]$ by $\pm(k-1)$ in (20). Solving the resulting equation for k, we obtain the required number of steps for acquisition, k_{acq}, as

$$k_{acq} = \frac{\pm\frac{T}{N}\omega - \phi_{ss}}{2\pi - \omega T \pm \frac{T}{N}\omega} \tag{21}$$

In the above equation the upper or lower sign is taken depending on $\omega > \omega_o$ or $\omega < \omega_o$, respectively. Once k_{acq} has been determined, the acquisition time, T_{acq}, is readily obtained from

$$T_{acq} = \frac{\phi_{ss} + 2\pi k_{acq}}{\omega} \tag{22}$$

2. First-Order Loop with L ($L \geq 2$) Level Quantizer

In L-level quantization, the value of $Q[\sin\phi(j)]$ is taken to be 0,. ±1, ±2, ..., or $\pm L$. We assume that the probability of having each of those quantized values is the same until the DPLL becomes in lock condition, and that the quantizer used has no dead zone. The expected value of $Q[\sin\phi(j)]$ is then $\pm(L+1)/2$. Thus, if $\omega < \omega_o$,

$$\sum_{j=0}^{k-1} Q[\sin\phi(j)] = -\left(\frac{L+1}{2}\right)(k-1), \tag{23}$$

and if $\omega > \omega_o$,

$$\sum_{j=0}^{k-1} Q[\sin\phi(j)] = \left(\frac{L+1}{2}\right)(k-1). \tag{24}$$

Consequently, we obtain

$$k = \frac{\pm\frac{L+1}{2}\cdot\frac{T}{N}\omega - \phi_{ss}}{2\pi - \omega T \pm \frac{L+1}{2}\cdot\frac{T}{N}\omega}. \tag{25}$$

where the upper or lower sign is taken again depending on $\omega > \omega_o$ or $\omega < \omega_o$, respectively. As before, the acquisition time can be obtained by substituting (25) into (22).

3. Second-Order Loop with One-Level Quantizer

To obtain the analytical expression for acquisition time of the second order DPLL, we first find the output phase of the clock, $\theta_o(k)$, and then substitute this value into (13) to obtain t(k). Then, we obtain the number of steps required for acquisition by substituting t(k) into (19).

Introducing the transfer function D(z) of the loop filter given by (3) into (9), we obtain

$$\theta_o(k) = B\frac{z-E}{z-1}\sum_{j=0}^{k-1} Q\,[\sin\phi(j)], \qquad (26)$$

where

$$E \triangleq \frac{1}{1+a}$$

and

$$B \triangleq \omega_o \frac{T}{N}(1+a).$$

Multiplying (z-1) on both sides of (26), we can obtain the resulting equation in the following form:

$$\theta_o(k+1) - \theta_o(k) = B[\sum_{j=0}^{k} Q\,[\sin\phi(j)] - E\sum_{j=0}^{k-1} Q\,[\sin\phi(j)]]. \qquad (27)$$

As discussed previously, prior to phase locking, we have for a one-level quantizer

$$Q\,[\sin\phi(j)\,] = \pm 1 \text{ for } \omega \gtrless \omega_o.$$

Consequently, rearranging (27) yields

$$\theta_o(k) = \pm B\,(\frac{1-E}{2}\,k^2 + \frac{3E-1}{2}\,k - E). \qquad (28)$$

Substituting (28) into (13) and then the result into (19), we obtain a quadratic equation of k;

$$Xk^2 + Yk + Z = 0 \qquad (29)$$

where

$$X = \mp\frac{T}{2N}\omega a, \quad Y = \omega T - 2\pi \mp \frac{T}{2N}\omega \qquad (2\text{-a})$$

and

$$Z = \pm\frac{T}{N}\omega - \phi_{ss},$$

and the upper or lower sign is taken depending on $\omega > \omega_o$ or $\omega < \omega_o$, respectively. Solving (29) for k and taking only the positive sign since k is always a positive quantity, we have

$$k = \frac{-Y + \sqrt{Y^2 - 4XZ}}{2X} \qquad (30)$$

One should note that the k obtained above is not exactly the desired number of steps required for acquisition, k_{acq}. The reason is due to the filtering effect. This effect and a procedure of getting a correction term may be explained as follows. As discussed previously, since the DPLL under consideration is an all digital feedback system, no perfect locking is possible. The sampling instants alternate with respect to zero crossing points, and so does the phase error. Therefore, the outputs of the digital filter would oscillate about some value in the steady state. In the process of achieving the locking condition, the clock generates one pulse after the clock counts M pulses from the local oscillator, M being equal to $\omega_o N/\omega$. In this case the digital filter output would be N-M. Thus, one can say that the DPLL is in lock when the filter output oscillates about the value of N-M, and that the average value of one period of the filter output is also N-M.

When the absolute value of the second step of the digital filter is greater than or equal to M' (= | N-M |), the loop is in lock from the first step, and thus $k_{acq} = 1$. On the other hand, when the absolute value of the second step of the digital filter is less than M', the locking condition cannot be achieved instantly. Rather, it requires more than one step, the number of steps depending on M'. At the kth step in (30) the digital filter output is 2M' - (1+a). Several steps are required for this digital filter output to reduce to M'. The number of the required additional steps would be $2 + \frac{M'-2}{a}$. Therefore, the actual k_{acq} is

$$k_{acq} = k + (2 + \frac{M'-2}{a}) \qquad (31)$$

where k is obtained by (30).

4. Second Order Loop with L-Level (L≥2) Quantizer

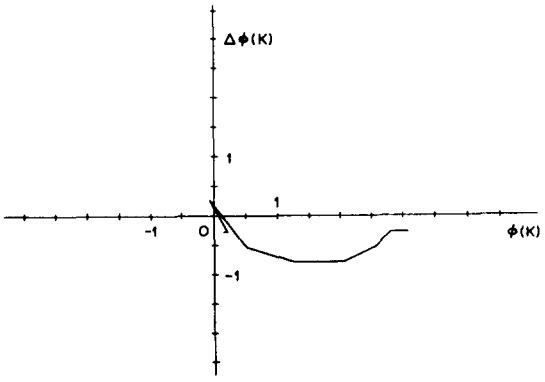

Fig. 10. Phase plane plot of first-order DPLL with phase error input [N = 24, L = 3, a = 0, $\theta_i(0)$ = 3.1 rad].

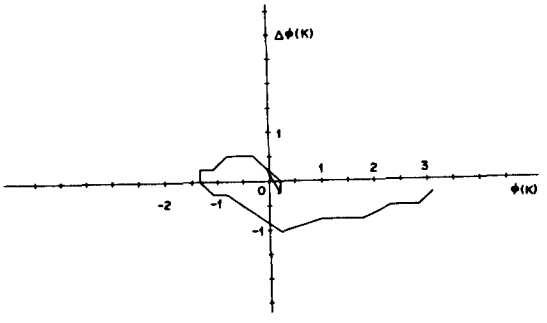

Fig. 11. Phase plane plot of second-order DPLL with phase error input [N = 24, L = 1, a = 0.5, $\theta_i(0)$ = 3.1 rad].

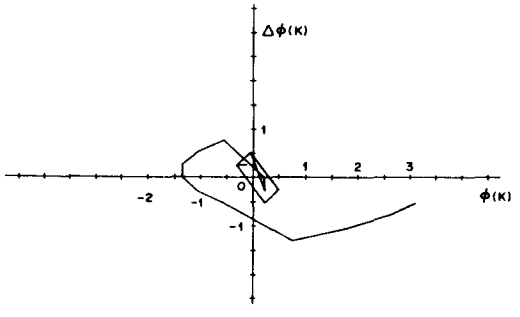

Fig. 12. Phase plane plot of second-order DPLL with phase error input [N = 24, L = 1, a = 1.0, $\theta_i(0)$ = 3.1 rad].

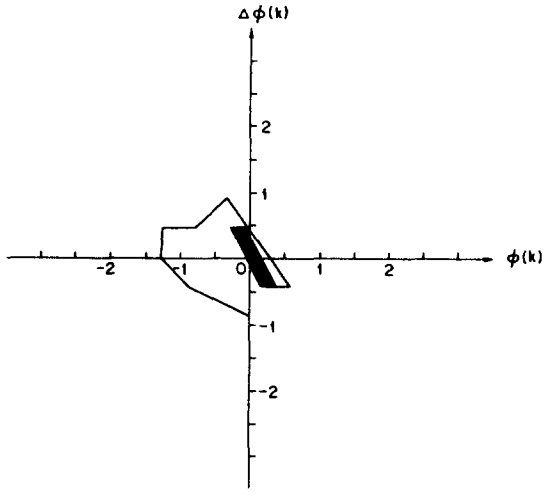

Fig. 13. Phase plane plot of second-order DPLL with frequency error input [N = 12, L = 1, a = 0.5, ω/ω_0 = 0.86].

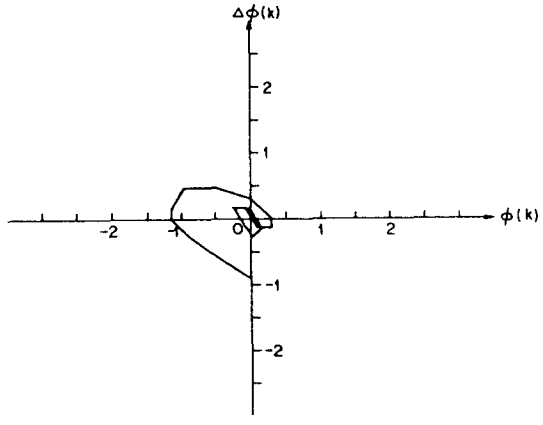

Fig. 14. Phase plane plot of second-order DPLL with frequency error input [N= 36, L=3, a=0.5, ω/ω_0 = 0.86].

Quantitative results of the acquisition time and range will be discussed in detail in the sections that follow.

IV. Acquisition Time of DPLL

Here we derive analytical expressions for acquisition time of the first- and second-order DPLL's. These results will be verified by computer simulation.

Analysis for $L \geqslant 2$ may be carried out in the same way as for the case of L=1. If the absolute value of the second step of the digital filter is greater than or equal to M', k_{acq} is then Q [sinφ(1).] Now consider the case of the absolute value of the second step of the digital filter is less than M'. As discussed previously in the case (C), we note that, before the DPLL is in lock, Q[sinφ(j)] = -L if $\omega < \omega_0$, and Q [sinφ (j)] = L if $\omega > \omega_0$. Hence, the quantities X, Y and Z defined in (29) must be modified as

$$X = \mp \frac{T}{2N} \omega aL, \quad Y = \omega T - 2\pi \pm \frac{T}{2N} \omega(2-a)\, L \tag{32}$$

and

$$Z = \pm \frac{T}{N} \omega L - \phi_{ss}.$$

With these modified quantities we can obtain k from (30).

In contrast to the case (3) [L = 1] in which several steps are required to reduce the absolute value of the digital filter output to M', we note in this case that, since the quantizer has several levels, the number of required steps for reducing the absolute value of the filter output to M' is very small (typically 1 or 2). Therefore, we neglect the correction term. Then, the required number of steps for acquisition, k_{acq}, in this case is equal to k that may be obtained from (30) and (32).

Needless to say, to obtain the acquisition time in all four cases, one needs to substitute k_{acq} in (22). Analytical and simulation results for a second-order DPLL systems are shown in Figs. 15 and 16. We observe from the Fig. that as the filter parameter, a, and the number of quantization levels, L, increase, acquisition time decreases.

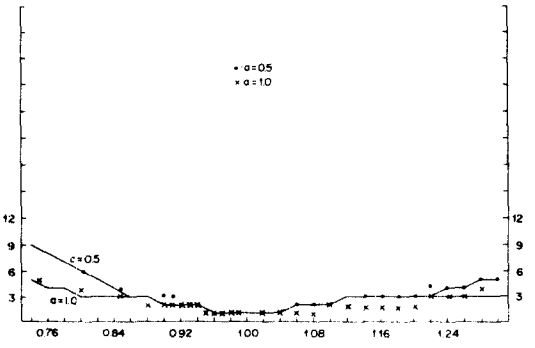

Fig. 15. Number of steps required for second-order DPLL to achieve locking vs. frequency deviation ω/ω_0 [N = 24, L = 1] (Solid line is theory and dotted points are simulation results).

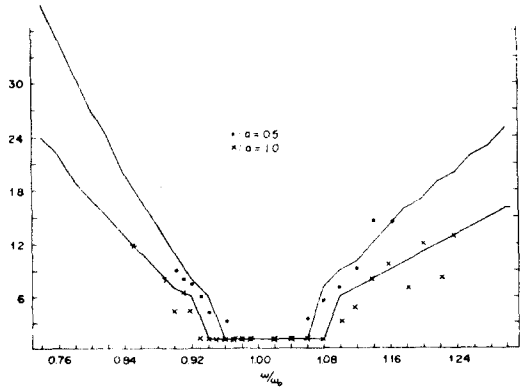

Fig. 16. Number of steps required for second-order DPLL to achieve locking vs. frequency deviation ω/ω_0 [N = 24, L = 3] (Solid line is theory and dotted points are simulation results).

V. Lock Range of DPLL

1. First-Order DPLL

We note that $\phi(k+1) \approx \phi(k) = \phi_{ss}$ in the steady state, and that the maximum and minimum values of $Q[A \sin\phi_{ss}]$ are L and -L, respectively. Hence, we obtain from (17) the following:

$$\frac{N}{N+L} \leqslant \frac{\omega}{\omega_0} \leqslant \frac{N}{N-L}. \tag{33}$$

This result is the same as that obtained first by Reddy and Gupta [2].

2. Second-Order Loop with One-Level Quantizer

First, consider the case that ω is less than ω_o. Locking procedure of a second-order DPLL with one-level quantizer is depicted in Fig. 17. We note that at the first step the digital filter output is zero, and the clock generates the first sampling pulse at the point P after it counts N pulses (See Fig. 17).

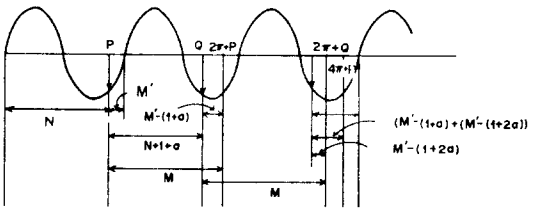

Fig. 17 Locking procedure of second-order DPLL with one-level quantizer.

Since the sign of the first sample is negative, the quantizer output of the second step is -1, and thus the digital filter output is $-(1+a)$, whose magnitude is less than M'. Thus, the second sampling point is on the left of the point, $2\pi+P$. If the absolute value of the digital filter output is equal to M', the second sampling point would be at the point, $2\pi+P$. If the absolute value of the digital filter output is greater than M', the second sampling point would be on the right of the point, $2\pi+P$. The above two cases arise when $k_{acq}=1$, as discussed in section IV. When the second sampling point is on the left of the point, $2\pi+P$, the quantizer output would be -1 at the third step. Then the digital filter output becomes $-(1+2a)$. In this case, since the absolute value of the digital filter output is less than M', the third sampling point is at $(2\pi+Q)$. In general, at the $(k+1)$ the step the digital filter output is $-(1+ka)$. The above process continues until the absolute value of the digital filter output is equal to M'. In this case the value of k is $\frac{M'-1}{a}$. After the $(\frac{M'-1}{a}+2)$ th step the absolute value of the digital filter output is greater than M'. Thus, if we assume that the previous sampling point is at some point, say R, the next sampling point is on the right of the point $2\pi+R$. Conseuqently, the DPLL would be in lock.

Now let us define a new quantity M'' as

$$M'' \triangleq M' - (1+a) + M' - (1+2a) + \cdots + M' - (1+\frac{M'-1}{a}\,a)$$

$$= \frac{M'^2 - (a+2)M' + a + 1}{2a} \tag{34}$$

If $M'' + M'$ is greater than $M/2$ at the kth step, the next sampling point would be on the left of the negative zero crossing, $2\pi(k-1)+\pi$. The quantizer output of the $(k+1)$th step is +1 and the DPLL cannot be in lock. However, if $M'' + M'$ is less than or equal to $M/2$, the absolute value of the digital filter output is greater than M', and the DPLL would be in lock. The above statement for locking condition may be reiterated algebraically as

$$M'' + M' \leqslant \frac{M}{2},$$

where

$$M' = \frac{N}{T}(\frac{1}{f} - \frac{1}{f_o}), \tag{35}$$

from which we obtain

$$\frac{N}{(N+a+1) + \sqrt{(N+a+1)^2 - (N^2+(2-a)N+a+1)}} \leqslant \frac{\omega}{\omega_o} \leqslant 1. \tag{36}$$

The inequality (36) represents the lower bound of the lock range of the second order DPLL with one level quantizer.

Next, we consider the case that ω is greater than ω_o. Since $f > f_o$, M' is equal to $\frac{N}{T}(\frac{1}{f_o} - \frac{1}{f})$. Thus, in this case the inequality (35) becomes

$$M'' + \frac{N}{T}(\frac{1}{f_o} - \frac{1}{f}) \leqslant \frac{M}{2}, \tag{37}$$

from which we obtain

$$1 \leqslant \frac{\omega}{\omega_o} \leqslant$$

$$\frac{N}{(N+a-1)-\sqrt{(N+a-1)^2-(N^2+(a-2)N+a+1)}}. \quad (38)$$

Having obtained the lower and upper bounds of the lock range, we obtain the overall lock range of the second order DPLL with one level quantizer:

$$\frac{N}{(N+a+1)+\sqrt{(N+a+1)^2-(N^2+(2-a)N+a+1}} \leqslant \frac{\omega}{\omega_0} \leqslant \frac{N}{(N+a-1)-\sqrt{(N+a-1)^2-(N^2+(a-2)N+a+1)}}. \quad (39)$$

Fig. 18 shows lock range versus filter parameter value with N as a parameter for a second-order DPLL with one-level quantizer. It is seen that, as the number of phase error states, N, decreases, the lock range increases. Also, it is observed that, as the filter parameter value, a, increases, the lock range increases. However, no significant increase can be attained beyond a = 2.

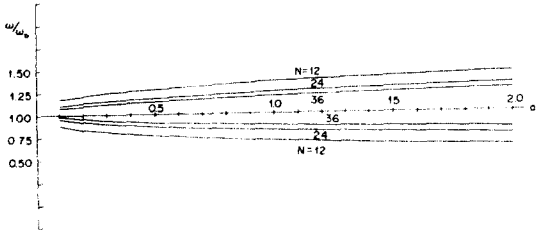

Fig. 18. Lock range of second-order DPLL with one-level quantizer vs. filter parameter value 'a'.

3. Second-Order Loop with L(L≥2) Level Quantizer

We first consider the case that ω is less than ω_0. The first sampling pulse from the clock is generated after $N\cdot\frac{T}{N}$ seconds from t(0), and the second sampling pulse is generated after $N + L(1 + a)\cdot\frac{T}{N}$ seconds from the time of the first sampling pulse (i.e., t(1)). Hence, the second sampling pulse is generated after $[2N + L(1 + a)]\frac{T}{N}$ seconds or $\omega[2N + L(1 + a)]\frac{T}{N}$ radians from the origin. At this time, the sampled output of the incoming sinusoidal wave is $\sin[\omega[2N + L(1 + a)]\frac{T}{N}]$. If M′ is less than L(1 + a), the DPLL would be in lock, but if M′ is greater than or equal to L(1 + a), it would be out of lock. In Fig. 19,

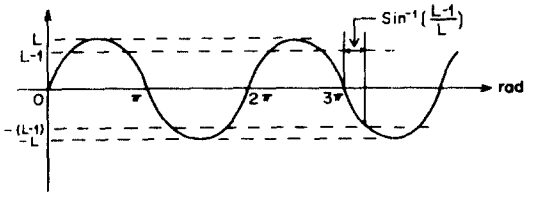

Fig. 19. Illustration showing $\sin^{-1}(\frac{L-1}{L})$.

if the second sampling pulse is generated between the points of the first sampling instant and 3π, it would be impossible to lock. Furthermore, if the second sampling pulse is generated between the points of 3π and $3\pi+\sin^{-1}(\frac{L-1}{L})$, it would be also impossible to lock, since the next quantizer output is less than or equal to L − 1, and thus the inequality $M' < L(1+a)$ cannot be satisfied. Therefore, for locking the point of the second sampling instant should be greater than or equal to the point of $3\pi + \sin^{-1}(\frac{L-1}{L})$. Writing this statement algebraically, we have

$$\omega[2N + L(1 + a)]\frac{T}{N} \geqslant 3\omega + \sin^{-1}(\frac{L-1}{L}), \quad (40)$$

which may be written in another form as

$$\frac{[1.5 + \frac{1}{2\omega}\sin^{-1}(\frac{L-1}{L})]N}{2N + L(1 + a)} \leqslant \frac{\omega}{\omega_0} \leqslant 1. \quad (41)$$

The inequality (41) gives the lower bound of the lock range of a second order loop with a multi-level quantizer.

Next, we consider the case that ω is greater than ω_o. To find the upper bound of the lock range, we use the similar argument. In this case we obtain

$$\omega[2N - L(1+a)]\frac{T}{N} \leqslant 5\pi - \sin^{-1}\left(\frac{L-1}{L}\right), \quad (42)$$

which may be rewritten as

$$1 \leqslant \frac{\omega}{\omega_o} \leqslant \frac{[2.5 - \frac{1}{2\pi}\sin^{-1}(\frac{L-1}{L})]N}{2N - L(1+a)} \quad (43)$$

Consequently, the lock range of a second-order DPLL with multilevel quantization is

$$\frac{[1.5 + \frac{1}{2\pi}\sin^{-1}(\frac{L-1}{L})]N}{2N + L(1+a)} \leqslant \frac{\omega}{\omega_o} \leqslant \frac{[2.5 - \frac{1}{2\pi}\sin^{-1}(\frac{L-1}{L})]N}{2N - L(1+a)} \quad (44)$$

Fig. 20 shows lock range versus filter parameter value with N as a parameter for a second-order DPLL with three-level quantization. Comparing Fig. 20 with Fig. 18, one can see that lock range increases as the number of quantization level increases.

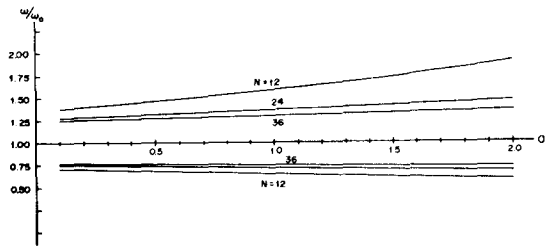

Fig. 20. Lock range of second-order DPLL with three-level quantizer vs. filter parameter value 'a'

VI. Conclusion

We have studied the acquisition behavior of a class of first- and second-order DPLL's commonly used in digital synchronization systems. Specifically, we have investigated the effects of quantization, filtering, and the number of phase error states on acquisition time and range. The acquisition behavior of the DPLL with different values of L, N and 'a' may be summarized as follows:

1) As the number of quantization levels, L, increases, acquisition time decreases, and lock range increases. Variation of L affects little the magnitude of the steady state phase error.
2) For a given L-level DPLL system, as N increases, acquisition time increases, and lock range decreases. However, in this case, the magnitude of the steady state phase error decreases, which is desirable. The steady state oscillating phase error is within the range of $\pm 2\pi/N$.
3) As in the analog counterpart, a first-order DPLL can not achieve locking at all times. For a second-order DPLL, one can get a smaller acquisition time and a larger lock range as the filter parameter value 'a' becomes larger. However, the magnitude of the steady state phase error increases in that case. Hence, a compromised value of 'a' must be taken.

The theoretical results obtained should be very useful in designing a DPLL.

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