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Performance Analysis and Design of FIR ADM Digital Filters

(FIR ADM 디지탈 필터의 性能 解析 및 設計)

鮮于鍾聲*, 殷鍾官**
(J. S. Sunwoo and C. K. Un)

要 約

본 논문에서는 적응 델타 변조기(ADM)를 A/D 변환기로 사용하는 FIR ADM 디지탈 필터의 성능과 구현 방법을 연구하였다. 이 필터는 지금까지 사용되는 PCM 필터와는 달리 승산이 필요 없을 뿐만 아니라 또한 저전력 소모, 크기 및 가격면 등에서 여러 가지 장점이 있다. 필터의 성능 해석을 위하여 필터의 mean-squared error의 식과 원하는 성능을 갖기 위한 필터의 word length의 식을 유도하였고 이를 computer simulation에 의해서 입증하였다. 또한 디지탈 필터의 성능을 최적화 하기 위해서 parameter 값들을 simulation에 의해서 최적화 하였다. 마지막으로 단일 및 다수의 신호를 동시에 처리할 수 있는 FIR ADM 디지탈 필터의 설계에 관해서 고찰하였다.

Abstract

Performance and realization of finite impulse response (FIR) digital filters that use an adaptive delta modulator (ADM) as an analog/digital converter have been studied. This filter requires no multiplication and offers many advantages over conventional PCM filters in low power consumption, small size, and cost effectiveness.

Analytical formulas have been derived for the expected mean-squared errors and also for the word length necessary to achieve the desired performance. Computer simultation has been done to optimize the parameter values and to verify the results of performance analysis. In addition, design of FIR ADM digital filters for processing single and multi-channel signals has been considered.

I. Introduction

In digital filtering pulse code modulation (PCM) is normally used for analog-to-digital (A/D) conversion of input signal. These PCM filters require multipliers, and consequently they are costly and consume a large amount of power. To avoid these problems, several researchers have studied a new type of finite impulse response (FIR) filter named delta modulation digital filter (DMDF). In a DMDF the input signal is digitized in one-bit word format, while in a conventional PCM digital filter the signal is digitized in multi-bit word

*正会員, 大韓電線(株)
**正会員, 韓国科学技術院 電気 및 電子工学科
(Dept. of Electrical Engineering, KAIST)
接受日字 : 1982年 3月 12日

format. Consequently, a DMDF does not need a multiplier in hardware realization since it requires only addition or subtraction operations.

The first significant study on FIR DMDF's was done by Peled and Liu.[1] They used linear delta modulation (LDM) to digitize the input signal. Recently, Lee and Un extended their work by deriving analytical formulas for the threshold word length and also for the optimum LDM step size of DMDF for various conditions.[2] Prezas and LoCicero considered the realization of a digital system that filters a DM encoded signal directly.[3]

Most related to the present study is Lawrence and Newcomb's work, in which they proposed a new type of FIR digital filter that uses adaptive delta modulation (ADM) to quantize the input signal.[4] In their scheme, an instantaneous adaptation algorithm was used, for which step size are powers of two, thereby eliminating multiplication operations. They used an analog lossy integrator and obtained filtered output in analog domain. The performance of their system has not been fully analyzed.

In this work, the performance and design criteria of FIR ADM filters are studied. Analytical expressions for the ADM quantization effect of input signal and the finite register length effect on the digital output are obtained in closed forms. Following this introduction, the FIR ADM digital filter under study is described in Section II. In Section III the performance of the ADM DF is analyzed by obtaining the mean-squared error (MSE) of the filter, and a formula for the filter threshold word length is obtained. In Section IV, to verify the analytical results of the ADM DF performance, computer simulation is done. In Section V we consider hardware implementation of the ADM DF system. Design of a special purpose digital signal processor for filtering multi-channel signals is also considered. Finally, conclusions are made.

II. Description of FIR ADM Digital Filters

A causal N-th order FIR digital filter is characterized by an input-output relationship of the form

$$y(k) = \sum_{i=0}^{N-1} h(i)\, x(k-i) \qquad (1)$$

where $\{x(k)\}$ and $\{y(k)\}$ are the input and output sequences, respectively, and $\{h(k)\}$ is the impulse response of the system.

Conventional implementation of a digital filter given by (1) is illustrated in Fig. 1. Here

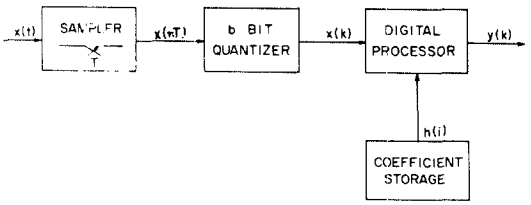

Fig. 1. PCM realization of a digital filter.

the analog signal is sampled and converted into a b-bit word. The PCM output sequence x(k) is fed to a digital processor to perform additions and multiplications, and the output samples $\{y(k)\}$ are computed according to (1).

Let us now consider the ADM DF system. Eq. (1) can be written in terms of differences between adjacent samples as follows:

$$\Delta y(k) = \sum_{i=0}^{N-1} h(i)\, \Delta x(k-i) \qquad (2)$$

where

$$\Delta y(k) \triangleq y(k) - y(k-1)$$

$$\Delta x(k) \triangleq x(k) - x(k-1).$$

From the above equation we can have an equivalent filter that works on the difference signal. One can clearly see that the feature of an ADM system that encodes the difference between the real and predicted signals can be used to achieve the same filtering operation as does by the PCM filter.

A block diagram of realization of the ADM DF is shown in Fig. 2. The filter consists of three major parts; an ADM A/D converter, a

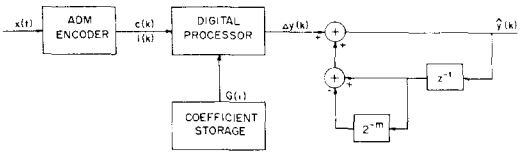

Fig. 2. ADM realization of a digital filter.

digital processor including a coefficient memory, and an accumulator. For A/D conversion of the input signal we use the constant factor DM(CFDM) approach. This method is similar to the one developed by Jayant,[5] but different in that the multiplication factors are 2 and 0.5 rather than 1.5 and 0.66 for ease of hardware implementation. In CFDM that is shown in Fig. 3 the binary signal b(k) is generated as

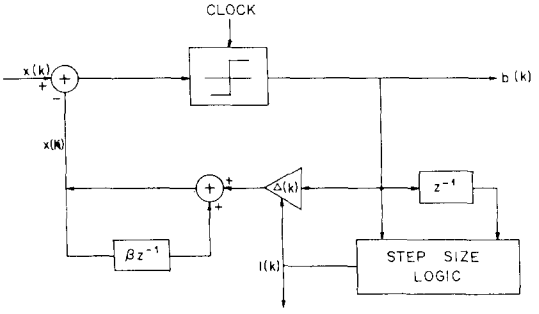

Fig. 3. Constant factor delta modulation encoder.

$$b(k) = \text{sgn}\{x(k) - \hat{x}(k)\} \tag{3}$$

$$\hat{x}(k) = \hat{x}(k-1) + \Delta(k)\, b(k-1) \tag{4}$$

where $\hat{x}(k)$ is the decoded sample at the k^{th} sampling time, and $\Delta(k)$ is the step size at the k^{th} sampling time given by

$$\Delta(k) = \Delta_{max} \cdot 2^{-\ell(k)}, \tag{5}$$

Δ_{max} being the maximum step size. The step size $\Delta(k)$ is controlled by the following logic rule:

$$\ell(k) = \begin{cases} \ell_{max} & , \text{if } b(k-1) \neq b(k-2),\ \ell(k-1) = \ell_{max} \\ \ell(k-1)+1, & \text{if } b(k-1) \neq b(k-2),\ 0 \leq \ell(k-1) < \ell_{max} \\ \ell(k-1)-1, & \text{if } b(k-1) = b(k-2),\ 0 < \ell(k-1) \leq \ell_{max} \\ 0 & , \text{if } b(k-1) = b(k-2),\ \ell(k-1) = 0. \end{cases} \tag{6}$$

Note that the minimum step size Δ_{min} is equal to $\Delta_{max} \cdot 2^{-\ell}$ max.

To obtain the equation by which the digital processor performs filtering operation, we replace $\Delta\hat{x}(k)$ by $\Delta(k)b(k-1)$ in (2) and use (5). We then have

$$\Delta\hat{y}(k) = \hat{y}(k) - \hat{y}(k-1) = \sum_{i=1}^{N-1} G(i) 2^{-\ell(k-i)}\, b(k-i-1) \tag{7}$$

where

$$G(i) = h(i)\, \Delta_{max}. \tag{8}$$

It is noted that b(k-i-1) gives only sign(i.e., +1 or -1), and that multiplication by $2^{-\ell(k-i)}$ is equivalent to shifting $\ell(k-i)$ bits to the right. All G(i)'s can be precomputed and stored in a read only memory (ROM). Hence, the digital processor can compute the increment of the DMDF output sequence, $\Delta\hat{y}(k)$, without multiplication operations by retrieving successively precomputed filter coefficients, shifting and then adding or subtracting the result from the accumulated sum.

Finally, the filtered output $\hat{y}(k)$ is obtained by feeding the incremental output $\Delta\hat{y}(k)$ to an accumulator. A digital leaky accmulator* can be implemented as follows. The transfer function of the accumulator is given by

$$T(z) = \frac{1}{1 - \beta z^{-1}} \tag{9}$$

where

$$\beta = e^{-T/\tau},$$

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* One can also use an ideal integrator or accumulator. In practice, however, because of its instability and performance degradation problems, a leaky accumulator is preferred.

T is sampling time interval and τ is the RC time constant of the corresponding analog leaky integrator. Since the leak factor β is close to but less than one, it can be written as

$$\beta \simeq 1 - 2^{-m} \tag{10}$$

where m is a constant showing the number of operations of shifting one bit. Hence, it is possible to realize the leaky accumulator without a multiplier by using a shift register and adders. The constant m can be chosen such that the leak factor β is nearest to the optimum value giving the best filter performance.

III. Performance Analysis of FIR ADM DF

Three different kinds of errors or noise are introduced in realization of an ADM DF. They are input quantization noise resulting from A/D conversion by ADM, errors due to finite word length of filter coefficients, and roundoff errors during shift and arithmetic operations. These are considered in this section.

One can write the predicted sequence x(k) of ADM as

$$\hat{x}(k) = x(k) + e_D(k), \tag{11}$$

where $e_D(k)$ is the ADM quantization noise sample of x(k). Also, the FIR filter coefficient G(i) $[=h(i)\,\triangle_{max}]$ rounded to b bits (including a sign bit) is given by

$$\bar{G}(i) = h(i)\,\triangle_{max} + e_Q(i) \tag{12}$$

where $e_Q(i)$ is rounding noise.
If we assume that the filter is causal, the actual output $\hat{y}(k)$ is from (2)

$$\hat{y}(k) = \sum_{i=0}^{N-1} G(i)\, x(k-i)/\triangle_{max}. \tag{13}$$

From (11), (12) and (13) the mean-squared error is

$$\begin{aligned} E[\epsilon^2(k)] &= E[\{\hat{y}(k) - y(k)\}^2] \\ &= E[\{\sum_{i=0}^{N-1} h(i)\, e_D(k-i)\}^2] \\ &\quad + E[\{\sum_{i=0}^{N-1} e_Q(i)\, \hat{x}(k-i)/\triangle_{max}\}^2]. \end{aligned} \tag{14}$$

In (14) the first term results from the in-band ADM quantization noise and the second term is due to filter coefficient quantization. If we assume that the input quantization error is negligibly small in amplitude compared with the input signal, (14) may be written as

$$\begin{aligned} E[\epsilon^2(k)] &= E[\{\sum_{i=0}^{N-1} h(i)\, e_D(k-i)\}^2] \\ &\quad + NN_Q R_{xx}(0)\,(1+\alpha)/\triangle^2_{max} \end{aligned} \tag{15}$$

where the rounding noise power N_Q is given by [6]

$$N_Q = 2^{-2b/3}, \tag{16}$$

$$\alpha = \frac{\sum_{i=0}^{N-1} R_{xx}(N-1-2i)}{NR_{xx}(0)}, \tag{17}$$

and $R_{xx}(\cdot)$ is autocorrelation of input sequence x(k).
Note that, since $R_{xx}(0) \geq R_{xx}(i)$ for all i, the magnitude of α is less than one. It results from the fact that for linear phase filters the coefficients are in pairs.

The in-band ADM quantization noise given by the first term of (15) requires an explicit expression in terms of various ADM parameters. In ADM systems, there are two types of quantization noise: granular noise N_g and slope-overload noise N_o. To obtain the total quantization noise N_D one may add them. Quantization noise of CFDM has been analyzed by Lee and Un.[7] We use their result in this study, which can be summarized as follows:

$$N_D = N_g + N_o, \tag{18}$$

$$\begin{aligned} N_g = \frac{8\triangle_g^2}{\pi^2 F_s} \Big\{ \frac{\pi^2}{12} + \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} (-1)^{ij} \\ \cdot \frac{\sin(2\pi i/F_s)}{2\pi i/F_s} \cdot \frac{1}{j^2} \exp\{-\frac{\pi^2 j^2}{\triangle_g^2}(1-a_i)\} \end{aligned} \tag{19}$$

$$N_o = \frac{1}{4\sqrt{2\pi}} \left(\frac{v_0^2}{v_2}\right) \left(\frac{3\sqrt{v_0}}{\triangle_0 f_s}\right)^5 \exp\left(-\frac{\triangle_0 f_s^2}{2v_0}\right) \quad (20)$$

where

$$\triangle_g = A(1-e^{-B\sigma}), \quad A(1-e^{-B\sigma}) \geq \triangle_{min} \quad (21)$$
$$= \triangle_{min}, \quad \text{otherwise}$$

$$\triangle_0 = \sqrt{v_0}/f_s \, \ell n F_s, \quad \text{if } \triangle_{min} \leq \triangle_0 \leq A$$
$$= A, \quad \text{if } \triangle_0 > A$$
$$= \triangle_{min}, \quad \text{if } \triangle_0 < \triangle_{min} \quad (22)$$

σ = rms value of x(t)
v_0 = variance of $x'(t)$
v_2 = variance of $x''(t)$

and B is an empirical constant. A is a constant related to the maximum allowable step size

$$A = (1 - \frac{1}{M}) \triangle_{max} \quad (23)$$

with

$M = 2\pi f_s / \sqrt{v_2/v_0}$
f_s = sampling frequency
F_s = ratio of sampling frequency to input bandwidth.

To determine the in-band ADM quantization noise, we assume that the FIR filter is a low-pass filter with its cutoff frequency smaller than the input signal bandwidth. Also, we assume that the power spectral density of granular noise is flat and that the cross-correlation coefficient between the input signal and the slope-overload noise is unity. Then, the in-band ADM quantization noise given by the first term on the right side of (15) is

$$N'_D = K(\gamma N_g + \delta N_o) \quad (24)$$

where K is an empirical correction factor,

$$\gamma = \sum_{i=0}^{N-1} \{h(i)\}^2 F_s/2 \quad (25)$$

$$\delta = \frac{\frac{1}{2\pi j} \oint X(z)H(z)Z(z^{-1})H(z^{-1}) \frac{dz}{z}}{\frac{1}{2\pi j} \oint X(z)X(z^{-1}) \frac{dz}{z}} \quad (26)$$

In (26) H(z) is the transfer function of the FIR ADM DF and X(z) is the z-transform of the input sequence.

Let us now discuss the roundoff errors occurring during the shift and arithmetic operations. We assume that fixed-point realization is done and that the sign-and-magnitude representation is used. In fixed point realizations the result of a shift should be rounded or truncated, but there is no need to do so in the case of addition (or subtraction). Here, the result of a shift is truncated to facilitate hardware realization. Fig. 4 shows finite-precision realization of the FIR filter. In this figure the effect of truncation is represented by the additive noise source e(•).

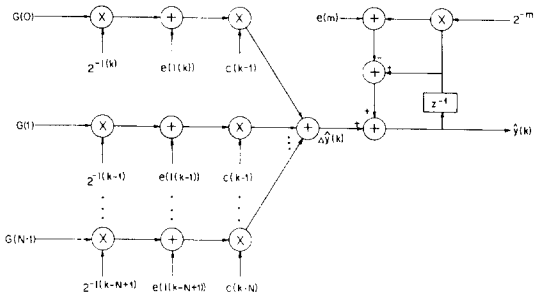

Fig. 4. Finite precision realization of an FIR filter.

When the number to be shifted is b bits, the variance of the truncation error is

$$E[\{e(n)\}^2] = \sum_{i=0}^{2^n-1} \frac{1}{2^n} (i \cdot 2^{-n-b+1})^2$$
$$= 4(1-2^{-n})(1-2^{-n-1}) \cdot N_Q \quad (27)$$

where n is the number of least signficant bits (LSB's) discarded after shifting and truncation. For convenience, one can divide the roundoff errors in two categories according to their sources. One category occurs during shifting operations for computation of the incremental output and the other occurs as a result of shifting for leaky integrator (accumulator).

To obtain a formula for the roundoff errors

of the first category, the actual filter coefficient may be written as

$$G(i) = h(i)\triangle_{max} + 2^{\ell(k-1)}\, e(\ell(k-i)). \quad (28)$$

Then, the mean-squared error at the output is given from (7) and (28) by

$$E[\{\epsilon(k)\}^2] = E[\{\hat{y}(k) - y(k)\}^2]$$
$$= E[\{\sum_{i=0}^{N-1} 2^{\ell(k-1)}\, e(\ell(k-i)) \cdot x(k-i)/\triangle_{max}\}^2]. \quad (29)$$

The average number of operations for shifting one bit can be expressed as

$$E[\ell(k-i)] = \log_2 \frac{\triangle_{max}}{\triangle_{eq}} \quad (30)$$

where $\triangle_{eq}$ is the equivalent step size. Then, the mean-squared error is simplified from (27) as

$$E[\{\epsilon(k)\}^2] = \frac{R_{xx}(0)}{\triangle_{eq}^2}\, 4N(1 - \frac{\triangle_{eq}}{\triangle_{max}}) \cdot (1 - \frac{\triangle_{eq}}{2\triangle_{max}})\, N_Q. \quad (31)$$

To obtain the information about the equivalent step size in (30), the statistical average step size used by Sakane and Steele may be used.[8] However, it has a clipping edge, and consequently does not yield a close agreement with the measured data. Therefore, we used a modified average step size given by

$$\triangle_{eq} = (P - \triangle_{min})(1 - e^{-Q\sigma}) + \triangle_{min} \quad (32)$$

where P and Q are constants that are exactly the same as those proposed by Sakane and Steele.

Let us now consider roundoff errors that occur during shifting operations in the leaky accumulator. The mean-squared value of the error at the output can be written as

$$E[\{\epsilon(k)\}^2] = E[\{\hat{y}(k) - y(k)\}^2]$$
$$= \frac{1}{2\pi j}\oint \frac{1}{1-\beta z^{-1}} \cdot \frac{1}{1-\beta z} \cdot E[\{e(m)\}^2]\, \frac{dz}{z}. \quad (33)$$

Note that β is approximately equal to $1-2^{-m}$. Using (27), we can write (33) as

$$E[\{\epsilon(k)\}^2] = \frac{2\beta}{1-\beta} N_Q. \quad (34)$$

Collecting the results (i.e., (15), (24), (31), and (34)), the total noise N_{total} introduced at the output may be written as

$$N_{total} = K(\gamma N_g + \delta N_o) + \frac{N}{\triangle_{max}^2} R_{xx}(0) \cdot (1+\alpha)N_Q + \frac{4N}{\triangle_{eq}^2} R_{xx}(0)(1 - \frac{\triangle_{eq}}{\triangle_{max}}) \cdot (1 - \frac{\triangle_{eq}}{2\triangle_{max}})\, N_Q + \frac{2\beta}{1-\beta} N_Q. \quad (35)$$

In (35), the first term results from the in-band ADM quantization noise, the second term is due to the filter coefficient quantization, and the last two terms represent the roundoff errors during the shifting operations.

Now, to obtain the formula for the threshold word length, we note that for a long word length the total noise given by (35) is dominated by the first term (i.e., ADM quantization noise). On the other hand, when the word length is short, the total noise consists mainly of the other three terms. The threshold word length b_{th} above which the system performs desirably can be obtained by setting the first term of (35) equal to the sum of the other three terms and then determining the word length. Noting that N_Q is equal to $2^{-2b}/3$, the threshold word length is given by

$$b_{th} = [\tfrac{1}{2}\log_2 (3N'_D/C)]_I + 1 \quad (36)$$

where

$$C = \frac{N}{\Delta^2_{max}} R_{xx}(0)(1+\alpha) + \frac{4N}{\Delta^2_{eq}} R_{xx}(0) \cdot \left(1 - \frac{\Delta_{eq}}{\Delta_{max}}\right)\left(1 - \frac{\Delta_{eq}}{2\Delta_{max}}\right) + \frac{2\beta}{1-\beta}, \quad (37)$$

and $[\cdot]_I$ represents the integer part of the quantity in the bracket.

IV. Computer Simulation Results of FIR ADM DF

For simulation we generated a flat bandlimited signal sampled at L times the Nyquist rate by filtering the random samples with a lowpass digital filter whose cutoff frequency is $f_s/2L$ (f_s is the sampling frequency). We have used elliptic filter that has eight poles. Also. we generated an RC shaped signal by passing bandlimited samples through a one-pole lowpass filter designed by the impulse invariant method. The ratio of the 3 dB attenuation point to the cutoff frequency was set to 0.23.[9]

To simulate an FIR ADM digital filter we chose a lowpass filter whose frequency response is shown in Fig. 5. The desired frequency characteristics are as follows:

Passband edge frequency	2.5 kHz
Stopband frequency	3.4 kHz
Passband ripple	0.47 dB
Stopband attenuation	45 dB

The number of filter coefficient was 60 for the sampling rate of 32 kHz.

In order to prevent overflow, the maximum root-mean-square (RMS) value of input signal was set to 0.25. The maximum step size was then obtained for the input signal level of σ= 0.25. The minimum step size was set to one thousandth of the maximum step size. Thus, the maximum number of bits shifted for computing the incremental output was 10, and the step size companding ratio was 60 dB.

The SQNR used as a performance measure here is defined as

$$SQNR = \frac{\sum_{i=1}^{N} \{y(i)\}^2}{\sum_{i=1}^{N} \{\hat{y}(i) - y(i)\}^2}$$

where N is the total number of input samples used in simulation. In our simulation, 6000

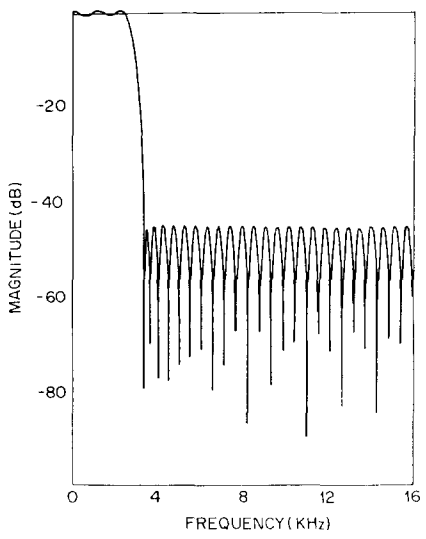

Fig. 5. Frequency response of an FIR ADM low-pass filter (f_s = 32 kHz).

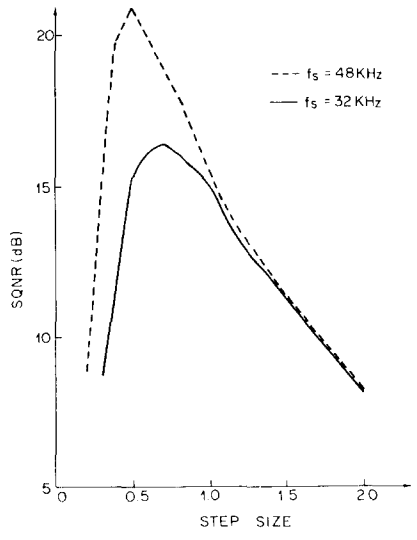

Fig. 6. Performance of LDM versus step size (RC-shaped Gaussian input signal was used.).

samples were used, but the first 1000 samples were discarded in obtaining SQNR to remove the initial transient effects.

We first obtained the optimum step size of LDM for the normalized input signal band-limited to 4 kHz at the sampling frequencies of 32 and 48 kHz. The result for the RC shaped Gaussian input is shown in Fig. 6. Then, the ADM system was simulated with the step size range of 60 dB. The maximum step size was set to ten times the optimum step size of LDM. Optimization of the accumulator time constant was done for the input signal with unity power. Fig. 7 shows variation

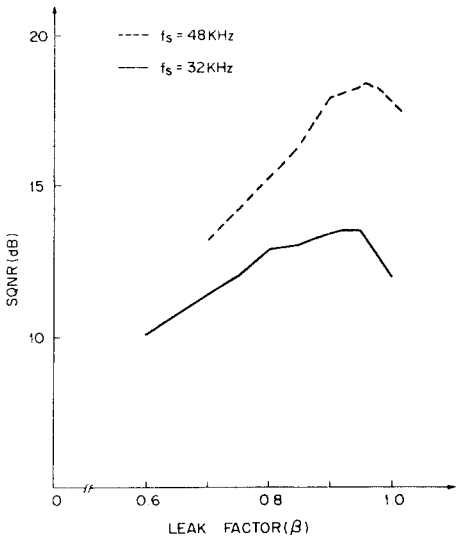

Fig. 7. Performance of CFDM versus leak factor (RC-shaped Gaussian input signal was used).

of ADM(CFDM) SQNR for different values of the leak factor. To facilitate hardware implementation we chose the best practical value of leak factor β in the neighborhood of the optimum value. The performance of CFDM with different leak factors (the optimum value, the actually used value, and unity) is shown in Fig. 8. With the non-optimum (actually used) leak factor, SQNR's of FIR ADM digital filters with different word lengths

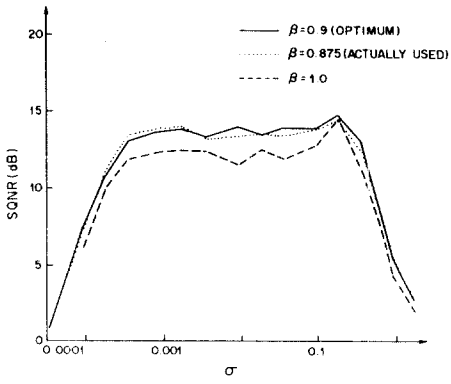

Fig. 8. Performance of CFDM versus rms input signal level σ (RC-shaped Gaussian input signal was used. $f_S = 32$ kHz).

(∞, 18, 16, 14, 12, 10 and 8 bits) were obtained. Fig. 9 shows the filter performance for the flat Gaussian input at different signal levels, and Fig. 10 shows the same for the RC shaped Gaussian input. In these figures the analytical results [Eq. (35)] obtained in Section III are also shown. One can see from those figures that the analysis and the simulation result agree closely.

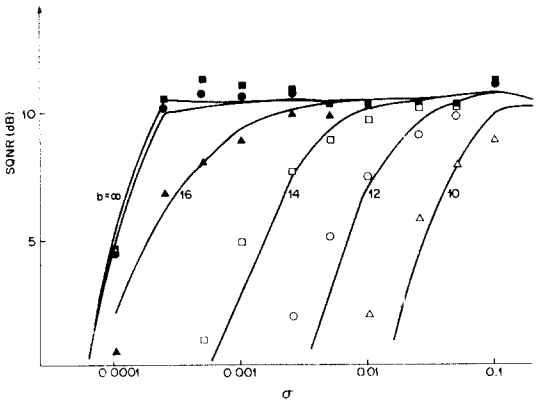

Fig. 9. Performance of FIR ADM digital filter versus rms input signal level σ for different word length b
(Flat Gaussian input signal was used. $f_S = 32$ kHz).

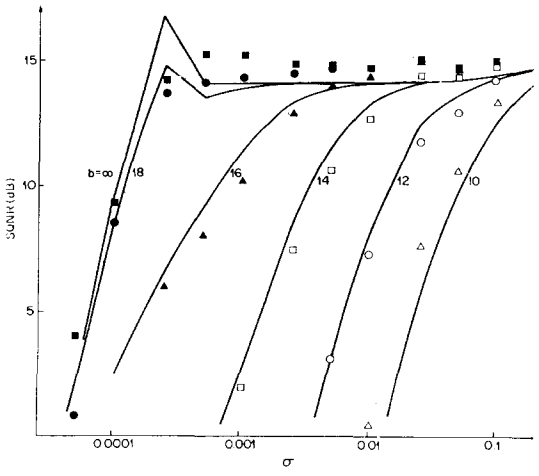

Fig. 10. Performance of FIR ADM digital filter versus rms input signal level σ for different word length b.
(RC-shaped Gaussian input signal was used. $f_s = 32$ kHz).

V. Consideration of Hardware Implementation

An FIR ADM digital filter hardware structure with serial mechanization is shown in Fig. 11, and realization of ADM coder is shwon in Fig. 12. The hardware may be divided into

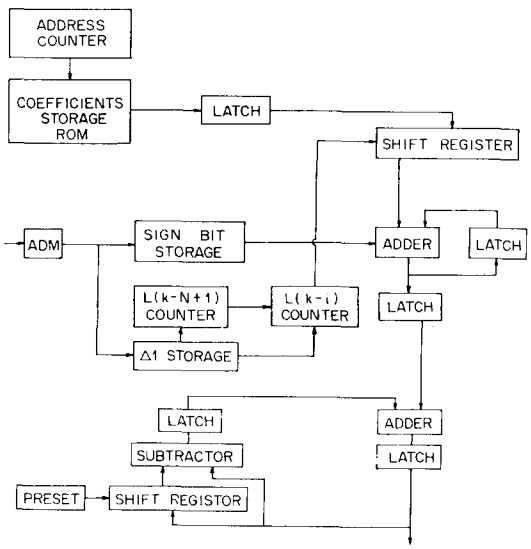

Fig. 11. Realizaton of FIR ADMDF hardware.

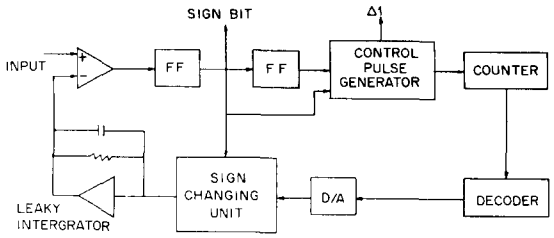

Fig. 12. Realization of ADM encoder.

four parts; an ADM coder, a digital processor, a coefficient storage unit and a leaky accumulator.

ADM coder consists of a one-bit quantizer and a feedback path containing the step size logic, a D/A converter, and an RC integrator. The ADM coder feeds the quantizer output binary stream and the relevant step size information to the digital processor. The step size information gives the control signal for counting direction of the up/down counter to control shift.

The digital processor is composed of shift registers, counters to control shift, an ALU for addition and subtraction operations, and latches. Data from the ADM coder is stored in shift registers and used for shifting and then adding or subtracting. Here, to store the binary signal coming from the ADM coder we can use a RAM. To accomplish the same operations as shift registers can, a synchronous presettable binary up-counter is used.

In the arithmetic section of the digital processor we require facility for subtraction as well as for addition. Only two-bit full adders are used, since the subtraction operation is accomplished by 2's complement addition.

Filter coefficients to be stored in ROM are represented in sign-and-magnitude notation. Here, all possible results of shifting operation may be precomputed and stored for hardware simplicity. However, this would require a large amount of storage. Since the FIR filter coefficients are symmetrical, only one half the coefficients are stored in ROM. The address counting

is done by using exclusive-OR gates.

The leaky accumulator consists of a shift register, two adders and latches. One adder and a shift register are used. Here, the shifting operation is accomplished by hardware connection without using a shift register. It is an efficient and simple realization.

The present digital filtering scheme is particularly useful in applications where several channels of information need to be processed by the same filter. The sampled signals of several channels can be multiplexed to form a string of samples. This string can then be processed by one common filter. At the output the channels can then be separated individually. By using this scheme the cost of the common digital hardware is shared by all the channels, so that the per-channel filtering cost can very well be economically competitive. Therefore, an FIR ADM digital filter is a reasonable alternative in applications where many voice or data signals need to be processed in the time-sharing mode by the same filter.

For multi-channel processing, hardware complexity does not increase significantly. Some data selectors/multiplexers are used and the expansion of the words of RAM storage is required. ADM-encode words of several channels are written into the allocated locations of RAM selected by the address. The content of the selected locations is fed to the arithmetic operator in the read mode. In arithmetic operation the incremental output is computed.

At the output the individual filtered samples are then separated or demultiplexed and stored in each allocated latch to be lessened and added with the incremental output. The hardware realization for filtering multiple-channel input signals is shown in Fig. 13.

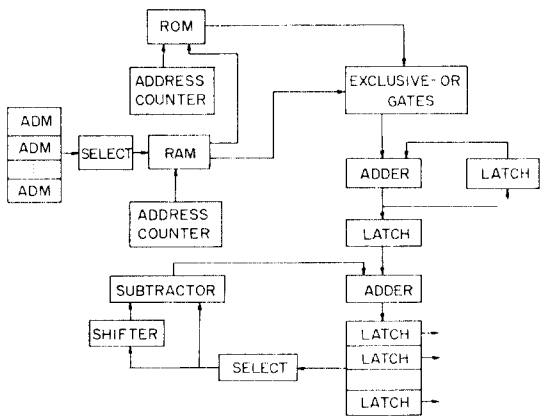

Fig. 13. Implementation of a multi-channel FIR ADM digital filter.

VI. Conclusions

In this work performance and realization of an FIR ADM digital filters have been studied. This filter can offer an attractive alternative to conventional PCM filters because of hardware simplicity and cost effectiveness. By having analysis and computer simulation of FIR ADM digital filters, we have obtained various design criteria of the filters. An efficient scheme of hardware realization that can be used for filtering speech signals has also been discussed. In addition, the filter hardware for processing multi-channel signals has been suggested.

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