論 文

論文 82-19-2-6

Analysis of Modified Digital Costas Loop Part I : Performance in the Absence of Noise

(變形된 디지탈 Costas Loop에 関한 研究 (I) 雜音이 없을 경우의 性能 解析)

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要 約

이 논문에서는 변형된 디지탈 Costas loop이라고 불리우는 새로운 형의 digital phase-locked loop (DPLL)을 제안하고 성능을 해석하였다. 제안된 DPLL의 주요 특성은 $\tan^{-1}(\cdot)$ 함수를 DPLL에 사용함으로써 phase error detector가 선형 특성을 갖게 되고, 따라서 mod-2π 선형 difference equation에 의해서 그 특성을 설명할 수 있다.

본 논문은 2부로 나뉘어져 1부에서는 먼저 제안된 시스템을 설명하고 잡음이 없는 경우 phase plane방법에 의해서 1차와 2차 loop의 성능을 해석했다. 초기 조건에 관계없이 locking이 될 수 있는 locking 범위의 식을 유도하고, 경우에 따라서 일어날 수 있는 false lock 또는 oscillation 현상을 설명했다. 이론적인 모든 해석은 컴퓨터 시뮬레이션에 의해서 입증되었다.

논문의 2부에서는 잡음이 있을 경우에 제안된 DPLL의 성능을 해석하였다.

Chapman-Kolmogorov 방정식을 사용하여 제안된 시스템의 phase error의 steady state probability density 함수, mean 및 variance를 얻었다. 이 결과들은 제2부에 게재 될 것이다.

Abstract

A new type of digital phase-locked loop (DPLL) called the modified digital Costas loop is proposed and analyzed. The main feature of the proposed loop is that the phase error detector of the loop has linear characteristic. This results from the use of the $\tan^{-1}(\cdot)$ function in the loop. Accordingly, the DPLL can be characterized by a modulo-2π linear difference equation.

This paper is divided into two parts. In Part I we describe the proposed system, and analyze the performance of the first- and second- order loops in the absence of noise by the phase plane technique. The locking ranges for the DPLL's to achieve exact locking independently of initial conditions have been obtained in closed forms. Also, the false lock and oscillation phenomena occurring under some initial conditions have been considered. These results have been verified by computer simulation.

In Part II we analyze the proposed system in the presence of noise. The steady state probability density function, mean and variance of the phase error have been obtained by solving the Chapman-Kolmogorov equation. These results will be presented in Part II.

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接受日字 : 1981年 12月 26日

I. Introduction

During the past two decades, analog phase-locked loops (APLL) have played an important

role in synchronous communication systems and many other applications. In recent years, as a result of the fast progress of digital integrated circuit technology, digital systems having many advantages over analog counterparts, such as high reliability, small size, lower cost and so forth, are rapidly replacing analog systems. Among these systems, digital phase-locked loops (DPLL's) are emerging as important digital subsystems.

Since the late 1960's, a variety of DPLL's have been proposed and analyzed[1-8]. A DPLL model that is essentially a discrete version of the conventional APLL was first proposed by Gill and Gupta[9, 10]. Since then, many research papers on this model have been published by others[11-14]. The behavior of Gill and Gupta's DPLL is characterized by a sinusoidal nonlinear difference equation. Because of this sinusoidal nonlinearity, it is difficult to analyze exactly the behavior of the system.

In this paper, a new type of DPLL called the modified digital Costas loop is proposed and analyzed. The proposed loop is characterized by a linear difference equation which has a mod-2π feature. Unlike other DPLL's, this system has a unique property in that the phase error detector characteristic is linear as a result of insertion of a $\tan^{-1}(\cdot)$ function in the loop. It is known[15] that the linear phase characteristic results in many attractive features in comparison with the conventional Gill and Gupta's DPLL. These include wider lock range and less stady-state phase error of the first-order loop for an input with frequency offset, less sensitivity of the convergence to initial phase errors for the second-order loop, and insensitivity of the locking conditions to variation of input signal power.

In the Part I of this paper we analyze the first- and second-order loops graphically by using phase plane plots, assuming that they are free of noise. Locking mechanism in the loops depends to a large extent upon the initial phase error conditions. False lock and oscillation phenomena occurring under some initial conditions are considered. The locking range for the loop to obtain exact locking independently of initial conditions is obtained in a closed form.

In the Part II of this paper the behavior of the first- and second-order-loops in the presence of noise is analyzed based upon the Chapman-Kolmogorov equation[16] When the input signal is corrupted by additive Gaussian noise, it has been found that the noise process in the loop becomes Pician as a result of inserting the $\tan^{-1}(\cdot)$ function in the loop for phase error detection. The steady state probability density function and variance of phase error are obtained.

Following this introduction, in Section II the modified digital Costas loop is described and its system equation is derived. In Section III the behavior of the first-order loop is analyzed in the absence of noise when there exists initial phase offset only and also when there exists frequency offset. In Section IV we analyze the second-order loop under the same conditions. Finally, we draw conclusions in Section V.

II. Description of Modified Digital Costas Loop

1. Structure of the Loop

A block digram of the modified digital costas loop is shown in Fig. 1. The loop is

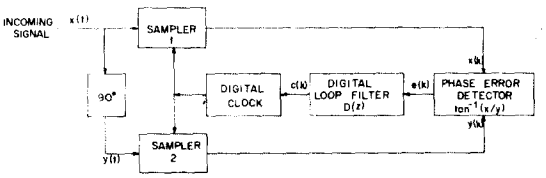


Fig. 1. Block diagram of modified digital Costas loop.

composed of a 90° phase shifter, two samplers, a phase error detector, a digital loop filter and

a digital clock as a voltage controlled oscillator (VCO). Of these subsystems, the first three form a phase detector and perform the function to detect phase error at sampling instants. Note that, unlike the conventional analog Costas loop[17], the quadrature signal of the proposed system is obtained by phase shifting the input signal rather than the digital clock output. Also the proposed loop is different from the conventional Costas loop in that it has a $\tan^{-1}(\cdot)$ function rather than a multiplier.

To detect the phase error at a sampling instant, the sampler 1 takes a sample x(k) from the input signal, and at the same time, the sampler 2 takes another sample y(k) from the 90° phase-shifted input signal. Then, phase error is obtained by getting a function of $\tan^{-1}[\frac{x(k)}{y(k)}]$. Detection of positive zero crossing is obtained by the sampler 1. Since the output of the phase error detector is equal to the phase error between the incoming signal and the digital clock at a sampling instant, its characteristic curve is linear as shown in Fig. 2.

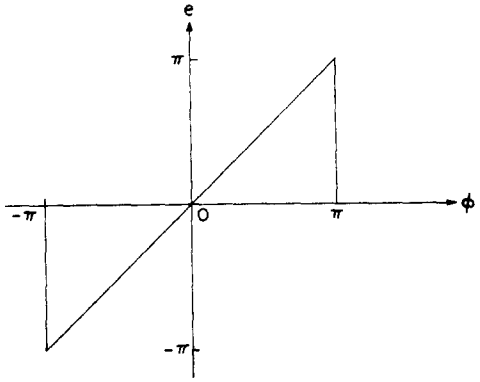


Fig. 2. Characteristic curve of phase error detector.

The behavior of the loop depends largely upon the transfer function of the digital loop filter D(z). The first-order loop filter has just a proportionality constant K, i.e., D(z)=K. For the second-order loop, we use the proportional-plus-accumulation filter given by

$$D(z) = a + \frac{b}{1 - z^{-1}}, \qquad (1)$$

where a and b are constants. The output of the digital loop filter provides a control signal to the digital clock for sampling. In our system the digital clock provides sampling time to the two samplers. The time interval between the k_{th} and $(k+1)_{th}$ sampling instants is controlled by the phase error at the k_{th} sampling time passed through the digital loop filter.

2. System Equation Describing the Loop Behavior

Let the incoming signals to the samplers 1 and 2 be x(t) and y(t), respectively, and assume that they are free of noise (i.e. n(t)=0). One can express x(t) as

$$x(t) = s(t) = \sqrt{2P_c}\ \sin[\omega_o t + \theta(t)], \qquad (2)$$

where P_c is the power of input signal s(t), ω_o is the free running frequency of the digital clock, $\theta(t)$ [$\triangleq \Delta\omega t + \theta_o$] is the phase process of s(t). Here $\Delta\omega$ is the initial frequency offset, θ_o is the initial phase offset, and ω[$\triangleq \omega_o + \Delta\omega$] is the frequency of the input signal. Also, since y(t) is a 90° phase-shifted signal of x(t), it is represented as

$$y(t) = \sqrt{2P_c}\ \cos[\omega_o t + \theta(t)]. \qquad (3)$$

When x(t) and y(t) are sampled, the sampled values x(k) and y(k) at the k_{th} sampling instant are given respectively by

$$y(k) = \sqrt{2P_c}\ \cos\phi(k), \qquad (4)$$

and $$x(k) = \sqrt{2P_c}\ \sin\phi(k), \qquad (5)$$

where $\phi(k) \triangleq \omega_o t(k) + \theta(k)$.

Then, the output of the phase error detector, e(k), is

$$e(k) = \tan^{-1}[x(k)/y(k)]. \qquad (6)$$

Note that in the noiseless case, e(k) is equal to $\phi(k)$. Consequently, the output of the

digital loop filter is given by

$$c(k) = D(z) \cdot \phi(k) . \tag{7}$$

where D(z) can be regarded as an operator. Since the interval T(k) between t(k) and t(k-1) is controlled by the control signal c(k), we have

$$T(k) = T_o - c(k-1), \tag{8}$$

where T_o is $2\pi/\omega_o$ representing a period of the digital clock. As an illustration, for the first-order loop with D(z) = K, the relationship between T(k) and $\phi(k)$ is shown in Fig. 3.

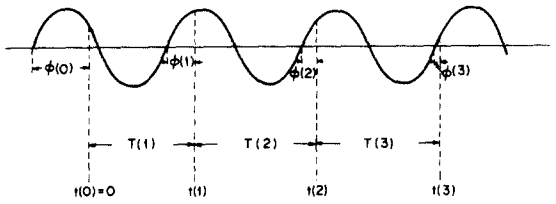


Fig. 3. Relationship between $\phi(k)$ and T(k).

In this case, c(k) is proportional to $\phi(k)$. The total time t(k) up to the k_{th} sampling instant is

$$t(k) = t(o) + \sum_{j=1}^{k} T(j)$$

$$= kT_o - \sum_{j=0}^{k-1} c(j) , \tag{9}$$

where t(o) has been assumed to be zero. Accordingly, $\phi(k)$ is given by

$$\phi(k) = \text{mod-}2\pi \, [\omega_o \, t(k) + \theta(k)]$$

$$= \text{mod-}2\pi \, [\theta(k) - \omega_o \sum_{j=0}^{k-1} c(j)]$$

$$= \Delta\omega \cdot kT_o + \theta_o - \omega_o \sum_{j=0}^{k-1} c(j) . \tag{10}$$

From the mathematical bases shown above, the difference equation characterizing the loop in the absence of noise can be derived as

$$\phi(k+1) = \phi(k) - \omega \cdot D(z) \, \phi(k) + 2\pi \cdot \Delta\omega/\omega_o . \tag{11}$$

This equation will be the basis of our analysis in the sections that follow.

III. Analysis of First-order Modified Digital Costas Loop

Here we consider the first-order loop behavior in the absence of noise for two different cases; the case of phase offset only and the case of frequency offset.

1. Case of Phase Offset Only

If we assume that the input signal has only phase offset (i.e., $\Delta\omega=0$), for the first-order loop the system equation (11) reduces to

$$\phi(k+1) = (1 - \omega_o K) \, \phi(k). \tag{12}$$

For convenience of analysis, we shall assume from now on that the free running frequency ω_o of the digital clock is normalized to unity. Then, from (12) the steady state phase error ϕ_{ss} must satisfy

$$\phi_{ss} = (1 - K) \, \phi_{ss}, \tag{13}$$

since $\phi(k+1) = \phi(k) = \phi_{ss}$ in the steady state. Accordingly, ϕ_{ss} must be zero.

Let us now consider the behavior of the loop for different values of K. Solving (12) for $\phi(k)$, we obtain

$$\phi(k) = (1-K)^k \, \phi(o), \tag{14}$$

where $\phi(0)$ is the initial phase error. Since $\phi(k)$ must be zero in the steady state, it is clear that the condition for the loop to be in lock is

$$| 1 - K | < 1. \tag{15}$$

Fig. 4 shows the phase plane plots for different values of K. Fig. 4 (a) shows the case for $0 < K < 1$ that results in monotonous locking. Fig. 4 (b) gives the plot for K=1 in which case locking occurs in one step. Fig. 4 (c) is the plot for $1 < K < 2$ representing the case of oscillatory locking. Fig. 4 (d) shows the case for $K > 2$. One can see that divergence occurs in this case. In these figures the initial phase point is represented by P_o, and subsquent

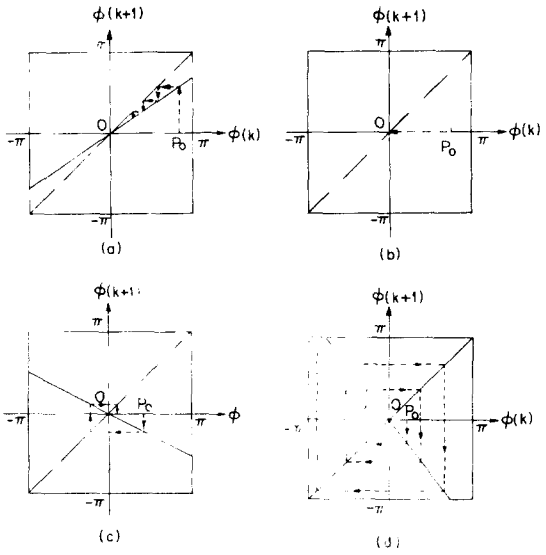


Fig. 4. Phase plane plots of first-order loop for different values of loop gain (ω=1).
(a) $0 < K < 1$ (b) $K = 1$
(c) $1 < K < 2$ (d) $K > 2$

points can be determined along the arrows.

2. Case of Frequency Offset

When the input signal has a frequency offset initially, the system equation becomes from (11)

$$\phi(k+1) = (1 - \omega K)\ \phi(k) + 2\pi\ (\omega - 1) \quad (16)$$

Since $\phi(k+1) = \phi(k)$ in the steady state, the steady state phase error ϕ_{ss} must satisfy

$$\phi_{ss} = (1 - \omega K)\ \phi_{ss} + 2\pi(\omega - 1), \quad (17)$$

from which we have

$$\phi_{ss} = \frac{2\pi}{K}\ (1 - \frac{1}{\omega}). \quad (18)$$

Note that, since $T(k) = T_o - K \cdot \phi(k-1)$ in the first-order loop, steady state clock interval T_{ss} becomes $\frac{2\pi}{\omega}$. Solving (16) for $\phi(k)$ by z-transform, we obtain

$$\phi(k) = \frac{2\pi}{K}\ (1 - \frac{1}{\omega}) + (1 - \omega K)^k \cdot [\phi(o) - \frac{2\pi}{K}\ (1 - \frac{1}{\omega})]. \quad (19)$$

Let us now consider conditions for the loop to achieve locking. Note from (19) that in order for $\phi(k)$ to converge as k becomes large, we must have

$$|\ 1 - \omega K\ | < 1. \quad (20)$$

Thus, the range of ω is given by*

$$0 < \omega < \frac{2}{K} \quad (21)$$

However, this condition is not sufficient for exact locking, because the system equation (16) must also be considered in the mod-2π sense.

Let us determine additional conditions by considering the behavior of the loop with the phase plane plots. Fig. 5 shows the phase

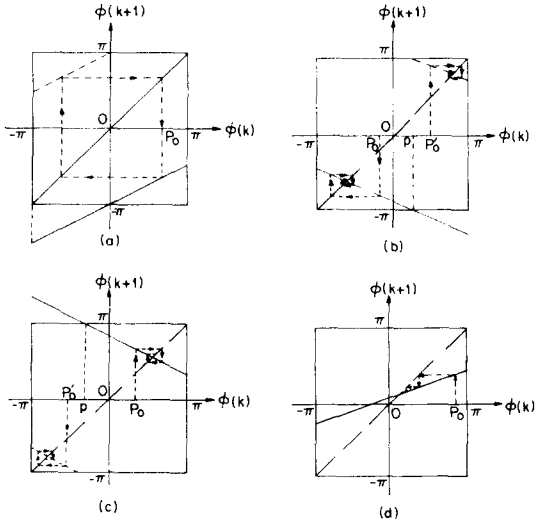


Fig. 5. Phase plane plots of first-order loop ($\omega \neq 1$).
(a) Oscillation
(b) and (c) clases of false locking
(d) Exact locking

* It should be noted that (21) is actually $0 < \omega/\omega_o < 2/K$. But, since ω_o has been normalized to unity, one can write the inequality as given in (21).

plane plots of four different cases. In this figure, the straight line corresponding to the system equation (16) is represented by the solid line. The solid line segment outside the rectangle must be shifted by 2π to be inside the rectangle because of the mod-2π property. Fig. 5 (a) shows the case of oscillation that occurs along the arrow because the steady state phase error does not exist in the interval $(-\pi, \pi)$. Fig. 5 (b) represents the phase plane plot for the case that false lock can occur under some initial condition. When the initial phase error is in the interval $(-\pi, p)$, the loop achieves exact locking. But, when it is in the interval (p, π), false lock occurs and the loop becomes locked at a frequency other than the desired frequency ω. Here, p can be interpreted as the boundary of initial phase error for false lock to occur. Fig. 5 (c) represents the case similar to Fig. 5 (b). The difference in this case is that the solid line has been shifted upwards. Thus, when the initial phase error is in the interval (p, π), the loop achieves exact locking. But, when it is in the interval $(-\pi, p)$, false lock occurs. Finally, in Fig. 5 (d) we show the case that solid line corresponding to the system equation (15) is inside the rectangle. In this case the loop achieves exact locking always independently of inital conditions.

From the above discussion it is clear that in addition to (21) the following three conditions must also be satisfied to achieve exact locking. First, the value of ϕ_{ss} must be in the interval $(-\pi, \pi)$. This condition is represented by

$$\left|\frac{2\pi}{K}\left(1-\frac{1}{\omega}\right)\right|<\pi, \tag{22}$$

from which we obtain

$$\frac{2}{2+K}<\omega<\frac{2}{2-K} \tag{23}$$

Second, when $\phi(k) = \pm\pi$, $\phi(k+1)$ must be in the interval $(-\pi, \pi)$. When $\phi(k) = \pi$, we must have.

$$|(1-\omega K)\pi+2\pi(\omega-1)|<\pi, \tag{24}$$

and consequently

$$0<\omega<\frac{2}{2-K} \tag{25a}$$

$$0<K<2. \tag{25b}$$

Also, when $\phi(k) = -\pi$, we must have

$$|-(1-\omega K)\pi+2\pi(\omega-1)|<\pi \tag{26}$$

or

$$\frac{2}{2+K}<\omega<\frac{4}{2+K}. \tag{27}$$

One may note that the phase plane plot shown in Fig. 5 (a) is for the case when the first condition, i.e., (23), is not met. Those shown in Fig. 5 (b) and (c) are respectively the cases when the second and third conditions, i.e., (25) and (27), are not satisfied.

Accordingly, from (21), (23), (25) and (27) the desired conditions to achieve exact locking independently of initial conditions are given as follows :

$$\frac{2}{2+K}<\omega<\min.\left[\frac{2}{2-K},\ \frac{4}{2+K}\right], \tag{28a}$$

and $0<K<2.$ (28b)

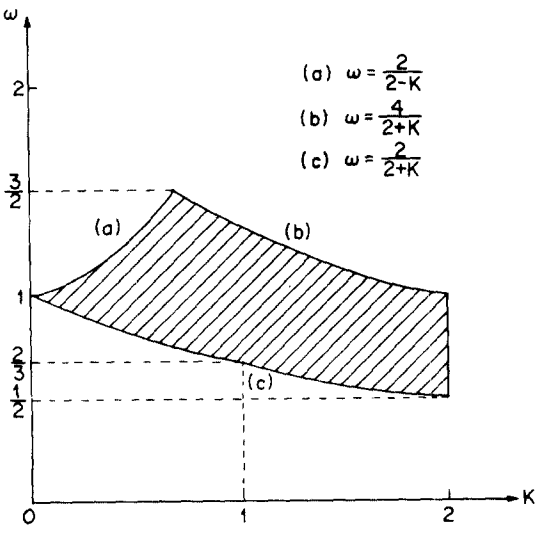


Fig. 6. Desired locking range of first-order loop.

The area enclosed by the inequalities (28) is ploted in Fig. 6.

Various simulation results for phase plane plots and steady state locking processes are shown in Fig. 7. Fig. 7 (a) shows the phase plane plot and the steady state locking process when the condition (23) is not met and thus oscillation occurs. Fig. 7 (b) shows the same when the condition (27) is not satisfied and consequently false lock occurs. Fig. 7 (c) shows the case when the desired locking conditions (28) are satisfied and thus exact locking is achieved always independently of initial condition.

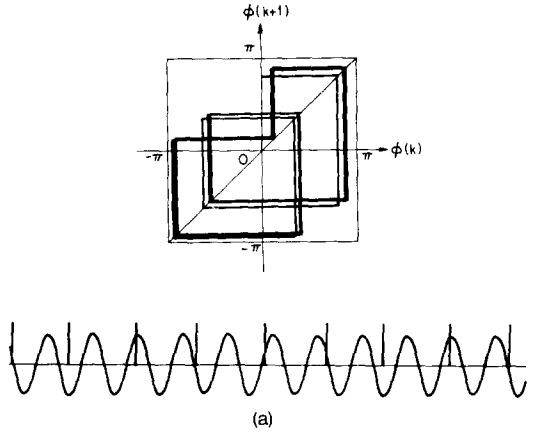


Fig. 7. Phase plane (top) and steady state locking processes (bottom) of first-order loop.
(a) Oscillation (ω = 1.4, K = 0.2 and P_O = 0)
(b) False locking (ω = 1.6, K = 1, P_O = 0)
(c) Exact locking (ω = 1.1, K = 1.2, Po = -2.5 rad)
(Locking always occurs independently of initial conditions.)

IV. Analysis of Second-order Modified Digital Costas Loop

We now analyze the performance of the second-order loop, assuming that the loop filter takes the form of the proportional-plus-accumulation filter given by (1). Again we consider first the case of phase offset only and then the case of frequency offset.

1. Case of Phase Offset Only

In this case the system equation becomes from (1) and (11)

$$\phi(k+2) = (2\text{-}a\text{-}b)\,\phi(k+1) - (1\text{-}a)\,\phi(k). \qquad (29)$$

In the steady state we have $\phi(k+2)=\phi(k+1)=\phi(k)$. Therefore, the steady phase error ϕ_{ss} must become zero to satisfy (29).

Now let us consider the locking conditions for the second-order loop. Taking z-transform of both sides of (29), one can obtain

$$\Phi(z) = \frac{\phi(0)z^2 + [\phi(1) - \phi(0)\cdot(2\text{-}a\text{-}b)]\,z}{z^2 - (2\text{-}a\text{-}b)z + (1\text{-}a)}, \qquad (30)$$

where $\Phi(z)$ is the z-transform of $\phi(k)$. First of all, note that for the loop to be locked, the roots of the denominator of (30) must be less than one. This requirement leads to

$$a > 0, \tag{31a}$$

$$b > 0, \tag{31b}$$

and $$2a + b < 4 . \tag{31c}$$

The region that satisfies (31) is the triangle (R_1, R_2, R_3 and R_4) shown in Fig. 8. These conditions, however, are not sufficient to guarantee the zero steady state phase error. In addition, the mod-2π feature of the linear difference equation (29) must also be considered.

Let us consider these additional conditions geometrically. In the case of the second-order loop, the phase plane plot can be considered in a three-dimensional space. For the second-order loop to achieve locking, i.e., to have the zero steady state phase error, the phase plane plot that may be obtained from (29) must pass through the inside of two planes $\phi(k+2) = \pm k$ in the region enclosed by four planes $\phi(k) = \pm k$ and $\phi(k+1) = \pm\pi$. In view of these properties, the following two conditions must be satisfied. First, when $\phi(k) = \pm\pi$ and $\phi(k+1) = \mp\pi$, we must have $|\phi(k+2)| < \pi$. This condition is represented by

$$|(2\text{-}a\text{-}b)\pi + (1\text{-}a)\pi| < \pi$$
$$\text{or } 2 < b + 2a < 4 \tag{32}$$

Second, when $\phi(k) = \pm\pi$ and $\phi(k+1) = \pm\pi$, we must have $|\phi(k+2)| < \pi$. This condition is represented by

$$|(2\text{-}a\text{-}b)\pi - (1\text{-}a)\pi| < \pi . \tag{33}$$

or $0 < b < 2$.

The regions enclosed by the inequalties (32) and (33) are R_3 and R_4 in Fig. 8. In these regions, the loop is locked to the zero steady state phase error.

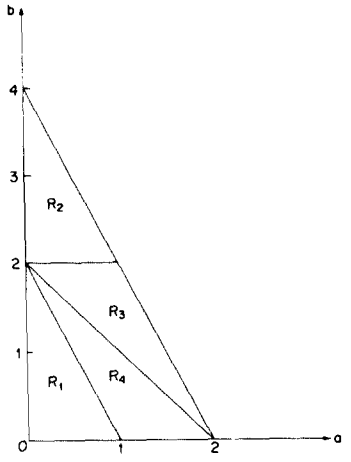


Fig. 8. Oscillation (R_1), non-zero steady state phase error (R_2), false locking (R_3) and exact locking (R_4) regions of second-order loop with initial phase offset only.

Let us now consider what happens when the above mentioned conditions (32) and (33) are not satisifed. First, we examine whether there exists a possibility that the loop may oscillate in the steady state between ϕ_{ss} and $-\phi_{ss}$ when the first condition (32) is not met (this case corresponds to the region R_1 in Fig 8.). We can have from (29) steady state phase errors ϕ_{ss} and $-\phi_{ss}$ such that

$$\phi_{ss} = -(2\text{-}a\text{-}b)\,\phi_{ss} - (1\text{-}a)\phi_{ss} + 2m\pi \tag{34}$$

holds, where m is an integer. Solving (34) for ϕ_{ss}, we have

$$\phi_{ss} = \frac{2m\pi}{4\text{-}2a\text{-}b} \tag{35}$$

In the case that (32) does not hold and thus $0 < b + 2a < 2$, there exists an integer $m=\pm 1$ for which $|\phi_{ss}|$ is not zero and less than π. Therefore, in the region R_1, we get a possibility that the loop may oscillate between ϕ_{ss} and $-\phi_{ss}$ for some initial conditions. Second, when the second condition (33) is not met (this case corresponds to the region R_2 in Fig. 8.), there exists ϕ_{ss} such that

$$\phi_{ss} = (2\text{-}a\text{-}b)\phi_{ss} - (1\text{-}a)\phi_{ss} + 2m\pi \qquad (36)$$

holds, from which we have

$$\phi_{ss} = \frac{2m\pi}{b} \qquad (37)$$

Because (33) does not hold, and thus $2 < b < 4$, $|\phi_{ss}|$ is again not zero and less than π for $m=\pm 1$.

Note that from (7) and (8), the difference equation relating to the sampling clock interval T(k) of the second-order loop is

$$T(k+1) = T(k) - (a+b)\,\phi(k) + a\phi(k-1). \qquad (38)$$

In this case, if $\phi_{ss} > 0$ (i.e., m=1), T(k) would decrease monotonously, and eventually becomes negative. This is unrealistic. Therefore, m can take -1 only. Consequently, ϕ_{ss} becomes $-\frac{2\pi}{b}$, and from (38), the difference between T(k) and T(k+1) is given by 2π. Thus, the sampling interval increases at the rate of one cycle per step in the steady state. As a result, in the region R_2, there exists a possibility that the loop may be locked to a non-zero steady state phase error for some initial conditions. Hence, for the loop to be locked to zero steady state phase error independently of initial conditions, a and b must take the values in the regions R_3 and R_4 in Fig. 8.

Consider now how the initial conditions affect the locking mechanism in the regions R_3 and R_4. Let z-transform of the loop filter output c(k) be C(z). Then, from (1), (7) and (30), C(z) is given by

$$C(z) = \frac{[(a+b)z - a]}{(z-1)} \cdot \frac{[\phi(o)z^2 + \phi(1) - \{\phi(o)\cdot(2\text{-}a\text{-}b)]\,z\}]}{[z^2 - (2\text{-}a\text{-}b)z + (1\text{-}a)]} \qquad (39)$$

Thus, the steady state value c_{ss} of c(k) is by the final value theorem of z-transform

$$c_{ss} = \lim_{z\to 1}(z\text{-}1)\ C(z) = \phi(1) + \phi(o)\cdot(a+b\text{-}1)\,. \qquad (40)$$

For the loop to be locked at the desired normalized frequency, the steady state value T_{ss} of the sampling clock interval T(k) must be $T_{ss}=T_o=2\pi$. Note that, since T(k) is T_o-c(k-1), T_{ss} is T_o-c_{ss}. Therefore, we must have $c_{ss}=0$. Thus, from (40), we have

$$\phi(1) = -\phi(0)\cdot(a+b-1)\,. \qquad (41)$$

For the loop to achieve correct locking, $\phi(0)$ and $\phi(1)$ must be in the interval $(-\pi, \pi)$. Since (41) represents a straight line on the plane of $(\phi(0)), \phi(1))$, $|\phi(1)|$ must be less than π for $\phi(0)=\pm\pi$. That is,

$$|\phi(1)| = |\pm\pi\cdot(a+b-1)| < \pi \qquad (42)$$

or $$|a+b-1| < 1. \qquad (43)$$

Thus, we have

$$0 < a + b < 2. \qquad (44)$$

Consequently, it can be concluded that, for the loop to be locked to the desired frequency ω_o independently of initial conditions, the inequalitities (32), (33) and (44) must be satisfied simultaneously. The region that satisfies these inequalities is R_4 in Fig. 8. If the loop filter parameter values a and b are chosen in the region of R_3 in the figure, the loop may be false-locked to a frequency other than the desired frequency ω_o with zero steady state phase error.

2. Case of Frequency Offset

We proceed in the same way as we analyzed in Sections III-B and IV-A. When initial frequency offset exists in the loop, the system equation becomes from (11)

$$\phi(k+2) = [2-(a+b)\omega]\,\phi(k+1) - (1-a\omega)\,\phi(k). \qquad (45)$$

Taking z-transform of both side of (45) and solving for $\Phi(z)$, we obtain

$$\Phi(z) = \frac{\phi(o)z^2 + [\phi(1) - \phi(o)\cdot\{2-(a+b)\omega\}]\cdot z}{z^2 - [2-(a+b)\omega]\ z + (1-a\omega)} \qquad (46)$$

As before, for the loop to be locked, the roots of the denominator of (46) must be less than one. To satisfy this condition, we must have the following inequalities :

$$a\omega > 0, \tag{47a}$$

$$b\omega > 0, \tag{47b}$$

and $$b\omega + 2a\omega < 4. \tag{47c}$$

Areas enclosed by these inequalities are plotted as regions R_1', R_2' and R_3' in Fig. 9. In addition, to guarantee zero steady state phase error, we must again consider the mod-2π feature of (45). As discussed in Section IV-A, to achieve locking to zero steady state phase error, the phase plane plot corresponding to (45) must pass through the inside of two plane $\phi(k+2)=\pm\pi$ in the region enclosed by four planes $\phi(k)=\pm\pi$ and $\phi(k+1)=\pm\pi$. Accordingly, the following two conditions must be satisfied. First, when $\phi(k)=\pm\pi$ and $\phi(k+1)=\mp\pi$, we must have $|\phi(k+2)| < \pi$. This condition is represented by

$$2 < (b+2a)\omega < 4. \tag{48}$$

Second, when $\phi(k)=\pm\pi$ and $\phi(k+1)=\pm\pi$, we must have $|\phi(k+2)| < \pi$. This condition is represented by

$$0 < b\omega < 2. \tag{49}$$

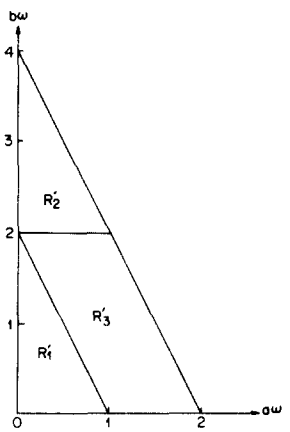


Fig. 9. Various locking regions of second-order with initial frequency offset.

The region R'_3 in Fig. 9 may be obtained from inequalities (48) and (49). In this region, the loop can achieve zero steady state phase error.

As in the case of phase offset only, consider now what happens if the conditions (48) and (49) are not satisfied. First, when the first condition (48) is not met (this case corresponds to the region R'_1 in Fig. 9), there exist ϕ_{ss} and $-\phi_{ss}$ such that

$$\phi_{ss} = -[2-(a+b)\omega]\phi_{ss} - (1-a\omega)\phi_{ss} + 2m\pi, \tag{50}$$

where m is an integer. In this case, ϕ_{ss} is given by

$$\phi_{ss} = \frac{2m\pi}{4-2a\omega a-b\omega} \tag{51}$$

In the case that (48) does not hold and thus $0 < a\omega + 2b\omega < 2$, there exists an integer $m=\pm 1$ for which $|\phi_{ss}|$ is not zero and less than π. Accordingly, in the region R'_1, there exists a possibility that the loop may oscillate between ϕ_{ss} and $-\phi_{ss}$ for some initial conditions. Second, consider the case that the second condition (49) is not met. This case corresponds to the region R'_2 in Fig. 9. In this case, we can have ϕ_{ss} such that

$$\phi_{ss} = [2-(a+b)\omega]\phi_{ss} - (1-a\omega)\phi_{ss} + 2m\pi, \tag{52}$$

where m is -1 for the same reason as discussed in Section IV-A. Thus, ϕ_{ss} is given by

$$\phi_{ss} = \frac{-2\pi}{b\omega} \tag{53}$$

From (38) and (53) the difference between the sampling clock intervals T(k) and T(k+1) in the steady state is given by $\frac{2\pi}{\omega}$. Accordingly, the sampling clock interval increases at the rate of one cycle per step. Therefore, in the region R'_2, the second-order loop may be locked to a nonzero steady state phase error for some initial conditions.

From the above discussion it is clear that

for the loop to be locked to a zero steady state phase error independently of initial conditions, $a\omega$ and $b\omega$ must take the values in the region R'_3 of Fig. 9. We now examine how the parameters a and b are related in the region R'_3. By taking the same procedure as to obtain (40), the steady state value of the loop filter output c(k) may be obtained as

$$c_{ss} = \frac{\phi(1) + \phi(0) \cdot [(a+b)\omega - 1]}{\omega} \qquad (54)$$

As discussed above, when the loop is locked at the desired frequency ω, the sampling clock interval T_{ss} in the steady state is $\frac{2\pi}{\omega}$. Also, note that T_{ss} is $T_o - c_{ss}$. Therefore, c_{ss} must be $T_o - \frac{2\pi}{\omega}$ or $2\pi(1-\frac{1}{\omega})$. Thus, from (54) we have

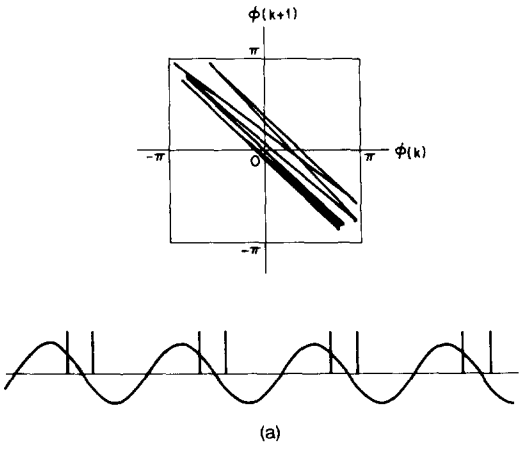
$$\phi(1) = 2\pi(\omega - 1) - \phi(0) \cdot [(a+b)\omega - 1] \qquad (55)$$

As before, when $\phi(0)=\pm\pi$, $|\phi(1)|$ must be less than π. Consequently, we obtain

$$2 < (a+b+2)\omega < 4, \qquad (56a)$$

and $$0 < (2-a-b)\omega < 2. \qquad (56b)$$

Note that the conditions (56) include the condition (44) as a special case of $\omega=1$. Therefore, for the loop to be locked at the desired frequency ω independently of initial conditions, the inequalities (48), (49) and (56) must be satisfied simultaneously. In other words, $a\omega$ and $b\omega$ must take the values in the region R'_3 in Fig. 9 and also satisfy (56). Otherwise, the loop may be false-locked at a frequency other than the desired frequency



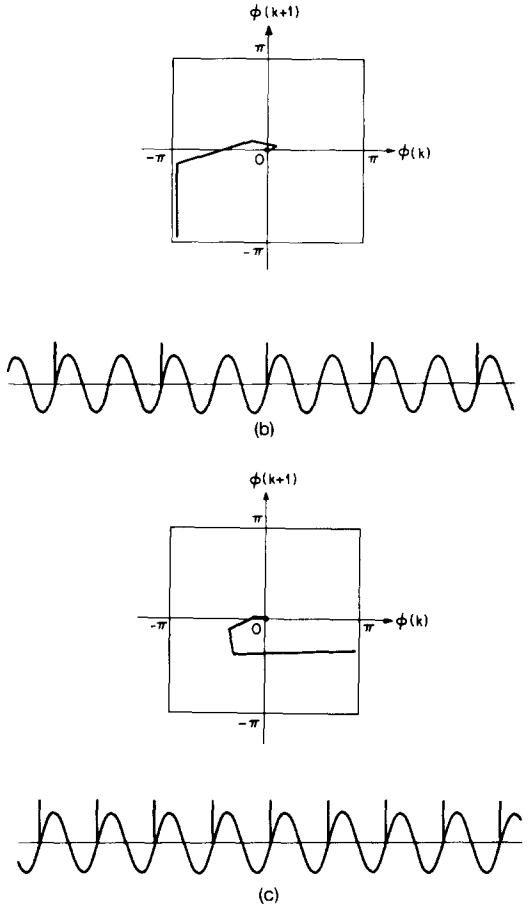


Fig. 10. Phase plane plots (top) and steady state locking processes (bottom) of second-order loop.
(a) Oscillation (ω = 0.477, a = b = 1.0472, P_o = -3 rad)
(b) False locking (ω = 1.2, a = b = 0.7, P_o = -3 rad)
(c) Exact locking (ω = 1.1, a = b = 0.7, P_o = 3 rad)
(Locking always occurs independently of initial conditions.)

ω for some initial conditions.

Various simulation results for phase plane plots and steady state locking process are shown in Fig. 10. Fig. 10 (a) represents the case when (48) is not satisfied and so oscillation occurs. Fig. 10 (b) represents the case when (48) and (49) are satisfied, but not (56) and thus false lock occurs. Fig. 10 (c) depicts the case when (48), (49) and (56) are all met and thus exact locking occurs always independently of initial conditions.

Finally, let us determine the locking range of the second-order loop. This may be obtained from the inequalities considered above. From (48), (49) and (56), it can be shown that the desired locking range is

$$\max.\left[\frac{2}{b+2a},\ \frac{2}{a+b+2}\right] < \omega < \min.\left[\frac{4}{b+2a}, \frac{2}{b}, \frac{4}{a+b+2}, \frac{2}{2-a-b}\right] \quad (57)$$

V. Conclusions

We have studied a new type of DPLL called the modified digital Costas loop. The main feature of the loop is that the characteristic of its phase error detector is linear. This linear characteristic results from the use a $\tan^{-1}(\cdot)$ function in the loop. As a result of this linear property, the DPLL can be characterized by a mod-2π linear difference equation. And the sampling clock interval is controlled by phase error itself.

In the noiseless case, the first- and second-order loops have been analyzed by the phase plane technique. Locking ranges of the loops have been obtained in closed forms. It has been found that oscillation and false lock occur depending on some initial conditions. Conditions for these phenomena have been obtained, and confirmed by computer simulation.

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