Performance Analysis of Extended n − Δ Delay-Lock Loops

(n − Δ Delay-Lock Loops 의 性能 解析)

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要 約

Delay-lock loop (DLL)는 相互關聯이 있는 두 波形 사이의 遲延差異를 追跡하는 한 最適裝置이다. 本 論文에서는 遲延時間이 n − Δ로 확장된 한 DLL의 구조와 同期喪失 주파수等 低域周波數帶의 性能이 解析되었다. 本 DLL은 correlator와 개선된 PN 신호장치로 구성되었으며, 相關特性은 확장된 S−커브의 형태를 가지고 있다. 雜音이 크더라도 追跡範圍와 初期同期時間이 좋은 特性을 가지고 있다. 3 − Δ DLL을 1 − Δ DLL과 비교하면 直列同期方式에서 初期同期時間이 3倍나 빠르며, doppler shift에 대한 저항이 2倍나 큰 것으로 나타났다.

Abstract

The delay-lock loop (DLL) is a statistically optimum device for tracking the delay difference between two correlated waveforms. In this paper an extended n - Δ (n=1,2,3, ...) DLL is described, and its baseband performance including the frequency to lose lock is analyzed. The present DLL system employs a correlator and a pseudonoise sequence synthesizer that has been improved from the previously used ones. The shape of the correlator characteristic has the form of expanded S-curve. Despite of increase noise, this extended DLL has desirable characteristics in tracking range and initial synchronization time. Comparing a 3 - Δ DLL with a 1 - Δ DLL, the former gives three times faster initial synchronization time with the serial synchronization method, and gives two times immunity against doppler shift.

I. Introduction

The delay-lock loop (DLL) is a statistically optimum device for tracking the delay difference between two correlated waveforms, and is used in many applications, such as spread spectrum communications, ranging, and radar systems.

Its basic properties have been described by Spilker and Magill [1]. Thereafter Spilker proposed and investigated a baseband DLL for binary signals [2]. A variety of implementation possibilities was considered for RF applications by Gill [3]. The dither technique was introduced and its characteristics were determined by Hartmann [4], thereby solving the unbalance problem of the two multipliers in the correlator of DLL. Biederman and Holmes derived the first passage time of a first order DLL by using the Fokker-Planck equation [5]. In all previous investigations, researchers studied only one-bit (1 - Δ) and two-bits (2 - Δ) delayed DLL's. [The delay interval of n - Δ (Δ is one bit interval) is equivalent to the tracking range of a DLL system.]

In this paper, we analyze the performance of an extended n - Δ system, thereby generalizing the previous results. As will be seen later, we can use many well-known results of a conventional phase-locked loop (PLL) by considering an n - Δ DLL. Of course, by extending the reference delay time to have more

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than 2 - Δ, one can enlarge the tracking interval of a DLL. In our system we use a synthesized correlation function to obtain an expanded S-curve. Normally each correlation function must be weighted to satisfy the S-curve characteristic. In this case, white Gaussian input noise is also increased. To alleviate this undesirable effect, rather than multiplying the input signal by the reference signal directly, we first delay the input signal by r - Δ (r is an arbitrary integer), and then correlate with the output of the pseudonoise synthesizer. The results of two correlators are then added. Accordingly, one can synthesize the correlation function without linearly increasing the noise. The pseudonoise (PN) sequence is assumed to be a stationary, random process with zero mean, and the input noise is time independent.

Following this introduction, we describe the extended n - Δ DLL in section II. In section III we construct a linear model of the extended n - Δ DLL, derive an equivalent system equation, and obtain the variance of the output noise. In section IV the normalized phase plane plots are shown for the DLL's. In section V the frequencies to lose lock in the first order n - Δ DLL's are compared for n = 1,2,3, and 4. Finally, conclusion is made in section VI.

II. Description of the Extended n - Δ DLL

A block diagram of the extended n - Δ DLL that we propose is shown in Fig. 1. The solid line describes the 3 - Δ or 4 - Δ DLL, and the additional dotted line is for the 5 - Δ or 6 - Δ DLL. The overall concept is similar to that of a conventional DLL except the correlator and the pseudonoise code synthesizer. A conventional DLL has normally 1 - Δ or 2 - Δ of tracking range. To extend the tracking range to more than 2 - Δ, we use a synthesized correlation function. The shape of the correlator characteristic of an n - Δ DLL becomes an expanded s-curve. In the proposed DLL the input and the time delayed signals are corrected to generate an error signal. This error signal serves to keep the DLL to track the delay time, once the system has been locked on.

The PN code synthesizer that generates the re-

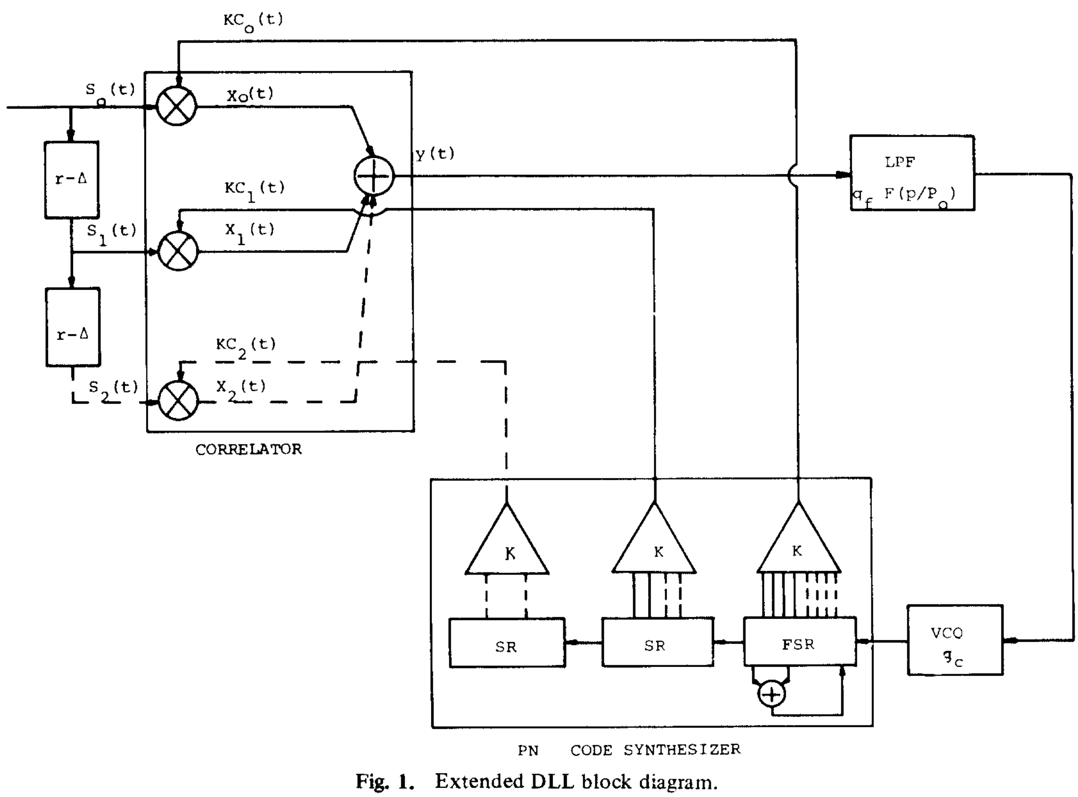

Fig. 1. Extended DLL block diagram.

ference signals consists of a maximal length linear feedback shift register (FSR), adders and shift registers. The number of shift registers depends on the order of delay n for an n - Δ DLL. In a conventional 1 - Δ or 2 - Δ DLL, the correlator is composed of two multipliers that multiply the input signal with two reference signals. If a synthesized reference signal is used as in our DLL system, we need only one multiplier. Consequently, the unbalance problem associated with the two multipliers is overcome, and the time sharing (dithering) technique normally used in a conventional DLL [4] is not needed.

As an example of the n - Δ system, let us consider the characteristic of a 3 - Δ correlator and its detailed circuit shown in Figs. 2 and 3, respectively. Note that the cross correlation of the input signal and a PN code output yields a triangular form. As shown in Fig. 3, $C_0(t)$ is composed of four time-delayed PN sequences, and $C_1(t)$ is composed of two time-delayed PN sequences which are initially delayed by a feedback shift register. The crosscorrelation functions that result from the multiplication of $S_0(t)$ by the four components of $C_0(t)$ are shown in Fig. 2 (a), and the sum of these correlation functions is shown in Fig. 2 (b). Also, the crosscorrelation functions that

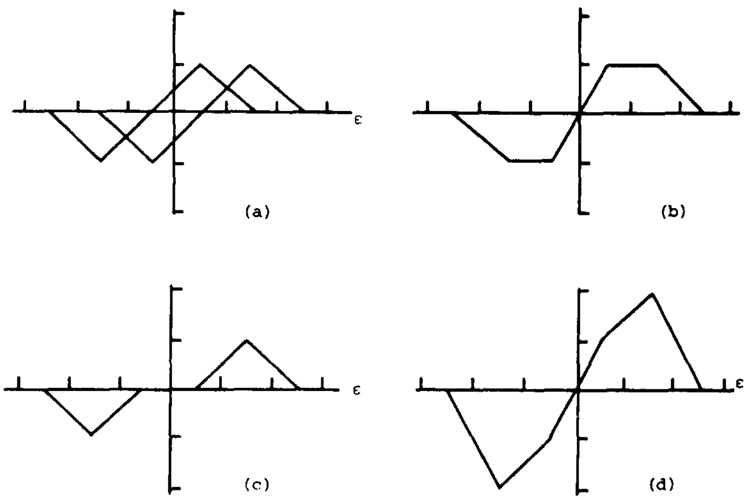

Fig. 2. Correlator characteristic of 3 - Δ DLL.

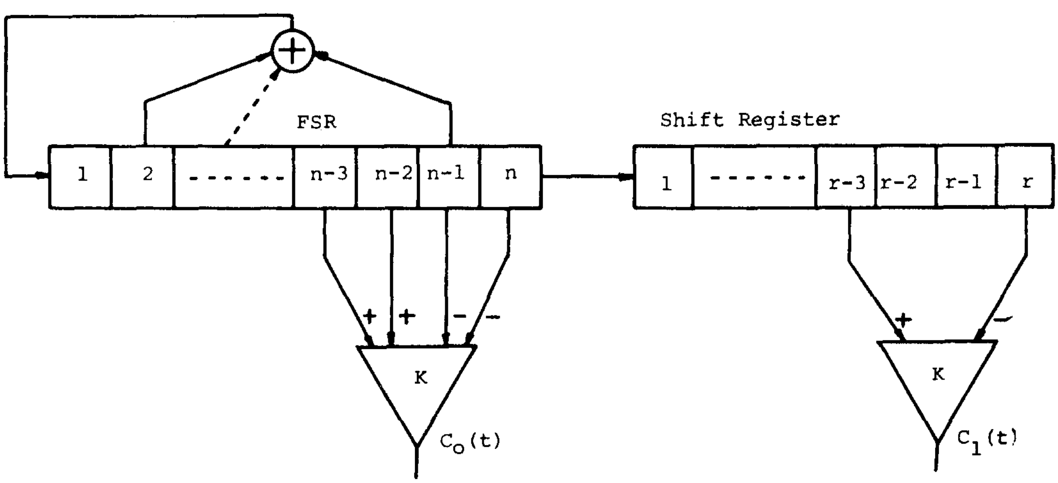

Fig. 3. 3 - Δ DLL PN code synthesizer.

result from the multiplication of the time delayed input signal $S_1(t)$ by $C_1(t)$ are shown in Fig. 2 (b). The characteristic of the 3 - Δ correlator is then obtained by adding the two sums of correlation functions, 2 (b) and 2 (c). This characteristic is shown in Fig. 2 (d). In this case, $C_0(t)$ is of five valued logic and $C_1(t)$ is of three valued logic.

The reference signal $C_j(t)$ in the n - Δ DLL is given by

$$C_j(t) = \sum_{k=0}^{m-j} \left\{ C\left[t + \left(\frac{n}{2} - k - rj\right)\Delta \right] - C\left[t - \left(\frac{n}{2} - k + rj\right)\Delta \right] \right\}, \quad j = 0,1,2,\cdots,m \tag{1}$$

where m is the integer part of (n-1)/2. The input signal may be written as

$$S_j(t) = \sqrt{P_s}\; C(t - rj\Delta) + n(t - rj\Delta). \tag{2}$$

C(t) is a maximal length PN sequence with the average power equal to one, r is an arbitrary integer to make the noise terms time independent, and P_s is the received signal power. The output of the correlator is obtained from (1) and (2) [see Fig. 1] as

$$\begin{aligned} y(t) &= K \sum_{j=0}^{m} C_j(t + \hat{T})\, S_j(t + T) \\ &= K\sqrt{P_s} \sum_{j=0}^{m} C_j(t + \hat{T})\, C(t - rj\Delta + T) \\ &\quad + K \sum_{j=0}^{m} C_j(t + T)\, n(t - rj\Delta + T), \end{aligned} \tag{3}$$

where K is the synthesizer gain; T and $\hat{T}$ are input and estimated delay time, respecitvely.

The first term of (3) may be divided into two parts; a term representing the nonzero mean correlator characteristic $D_n(\epsilon)$, and a zero mean self noise $n_s(t, \epsilon)$ [9]. The second term of (3) is the noise term, $n_n(t)$, generated from the input noise. Thus, we can write (3) as

$$y(t) = K[\sqrt{P_s}\; D_n(\epsilon) + n_s(t,\epsilon) + n_n(t)]\,. \tag{4}$$

Note that $D_n(\epsilon)$ is the statistical expectation of the correlator output y(t) and the mean values of the two noise terms are zero. The self noise, $n_s(t,\epsilon)$, generated by the correlator is negligible, when the signal to noise ratio (SNR) is much less than one, and the loop filter bandwidth is less than 1/2Δ [2]. Therefore, we neglect the self noise term in our analysis.

If we assume that the input noise is white Gaussian with one sided power spectral density of N_0, the output noise power spectral density for n - Δ DLL is

$$G_{nn}(f) = P_d N_0 \tag{5}$$

with $P_d = (m + 1)(m + 2)$,

where P_d is the average power of combined reference signals of PN codes. In the case of 3 - Δ DLL, the number of PN codes used is six, and thus P_d is six. Note that as the tracking range is increased, the noise power is also increased. But the noise variance of the present DLL system is rather small compared with that of the conventional DLL. This aspect is discussed in the next section.

III. Linear Model of the Extended DLL

Modeling of an equivalent system is essential in order to analyze the behavior of the nonlinear DLL system. Referring to Fig. 1, we can obtain the system equation of our DLL using (3) as

$$p\hat{T} = K g_c g_f F(p/p_0) \frac{M}{M + 1} [\sqrt{P_s}\; D_n(\epsilon) + n_n(t)]\,, \tag{6}$$

where K is the synthesizer gain, g_f is the loop filter gain, g_c is the VCO gain, M is the length of a maximal sequence, and p is the complex frequency variable. In general, M is much greater than one, and thus the coefficient of the crosscorrelation offset term, M/(M+1), is approximately equal to one. Hence, the system equation (6) can be written as

$$\frac{\epsilon}{\Delta} = \frac{T}{\Delta} - g_0 \frac{F(p/p_0)}{p} [\sqrt{P_s}\; D_n(\epsilon) + n_n(t)]\,, \tag{7}$$

with $g_0 = \dfrac{K g_f g_c}{\Delta}$, and $\epsilon = T - \hat{T}$.

This equation is similar in form to that of a conventional phase-locked loop (PLL). Therefore, using (7), we can have an equivalent linearized model as shown in Fig. 4. Note that the equavalent model of the generalized DLL is exactly the same as the linear model of a PLL. The equivalent signal amplitude A in the DLL model is determined by the slope of the correlator characteristic at the origin, $D_n'(0)$ For 1 - Δ and 3 - Δ DLL, $D_n'(0)$ is $2\epsilon/\Delta$, and thus, A is $2\sqrt{P_s}$. For 2 - Δ and 4 - Δ DLL, $D_n'(0)$ is ϵ/Δ, and therefore, A is $\sqrt{P_s}$. Since the transfer function is the same regardless of any n - Δ of DLL, the relative noise variances of n - Δ DLL's (n = 1,2,3,4, ...) are determined only by the equivalent signal amplitude A and the power P_d of the combined reference signals. For example, A and P_d of 1 - Δ DLL are given by $2\sqrt{P_s}$ and 2, respectively; and those of 4 - Δ DLL are $\sqrt{P_s}$ and 6, respectively (See Eq.(5)). The variances of various DLL's relative to the noise variance of the 1 - Δ DLL are shown in Table 1.

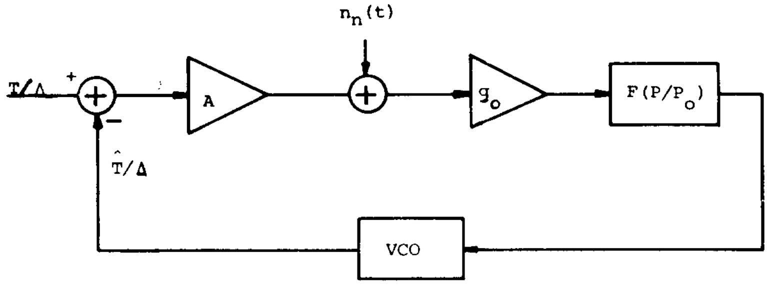

Fig. 4. Linearized model of extended n - Δ DLL.

The linearized model is exactly equivalent to the system equation (7), when the error signal is in the linear region. We can easily find the linear region from the correlator characteristic, $D_n(\epsilon)$. For example, 1 - Δ and 3 - Δ DLL have the linear region from -Δ/2 to Δ/2*; 2 - Δ has from -Δ to Δ; 4 - Δ has from -2Δ to 2Δ. From the above result, one can see that except the 3 - Δ DLL, the region where DLL is stable lies in the linear region. Thus, the use of the linearized model is justifiable for the operating system.

The noise variance of each DLL can be obtained from the linearized model, and may be expressed as follows [2];

$$\sigma_n^2 = \frac{\Delta^2 P_d N_o}{2A^2} \int_{-\infty}^{\infty} \left| H(j\omega/p_o) \right|^2 d\omega \qquad (8)$$

where H(•) is the transfer function of the equivalent model. The transfer function that is optimum (in the sense that it minimizes the total squared transient error plus the mean-squared error caused by interfering noise) for a ramp input of delay in the presence of white noise is given by [7]

$$H(p/P_o) = \frac{1+\sqrt{2}\, p/p_o}{1+\sqrt{2}\, p/p_o + (p/p_o)^2} \qquad (9)$$

Table 1. Relative variance of various n - Δ DLL'S.

	1 - Δ	2 - Δ	3 -Δ	4 -Δ	5 - Δ	6 -Δ
σ_n^2	1	4	3	12	6	24

Note that, in the case of the 3 - Δ DLL, the noise variance is smaller than the 2 - Δ DLL, while its noise power density is three times that of the 2 - Δ DLL. In the cases of 4 - Δ, 6 - Δ and higher n - Δ DLL's, the noise variance becomes very large, and thus it appears impractical to use them each as a tracking device.

IV. Phase Plane Plots

A phase plane plot of the nonlinear feedback DLL system is a convenient means to understand its acquisition characteristic. The phase plane plots

* One could consider the range between Δ/2 and 3Δ/2 as a linear region in 3-Δ DLL. However, we consider only the range between -Δ/2 and Δ/2 as a linear region in our analysis.

can be made by using the following differential equation which is obtained from the normalized system equation (7);

$$\frac{d\dot{x}}{dx} = -\frac{D_n(x) + [\sqrt{2}\,D_n'(x) + 1/g]\,\dot{x} - \dot{y}/g - \ddot{y}}{\dot{x}} \tag{10}$$

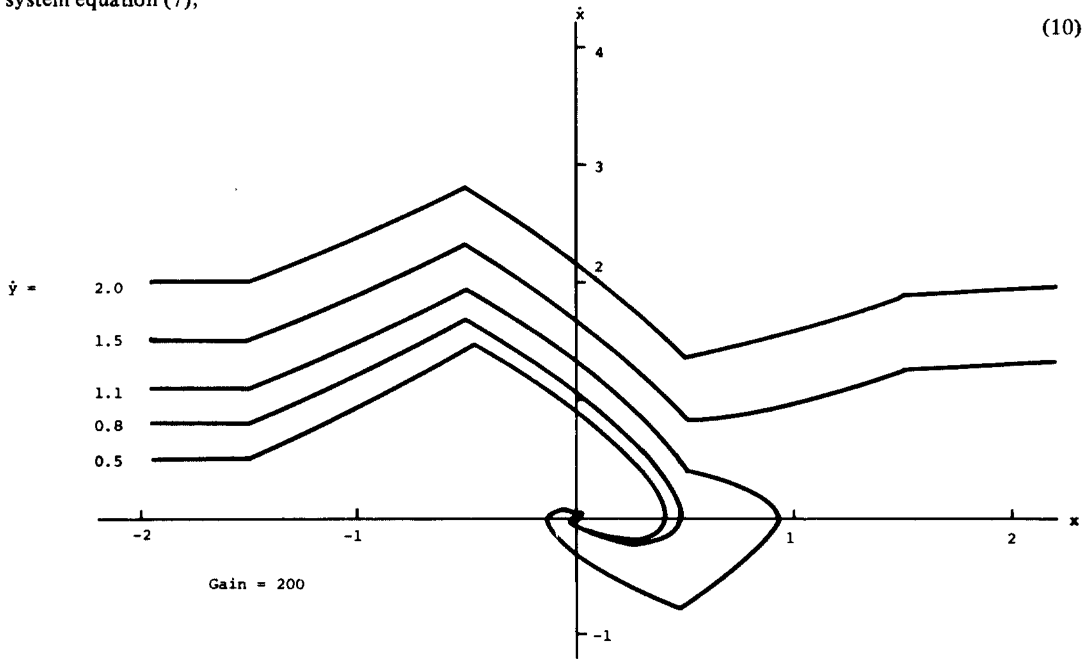

Fig. 5(a). Phase plane plot of 1 - Δ DLL.

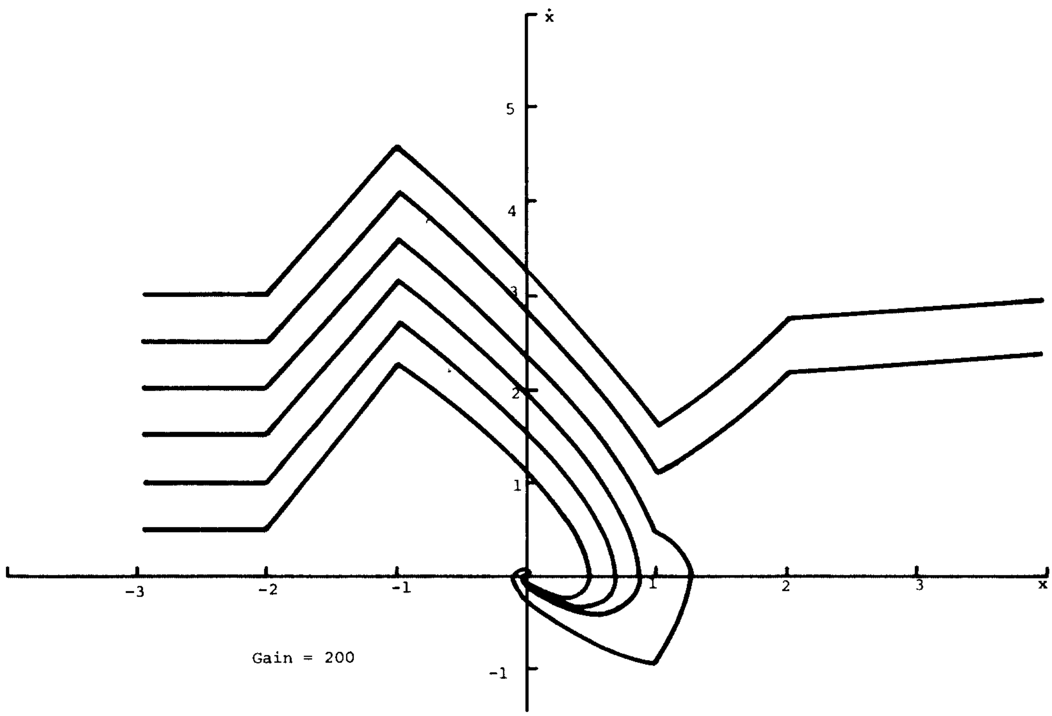

Fig. 5(b). Phase plane plot of 2 - Δ DLL.

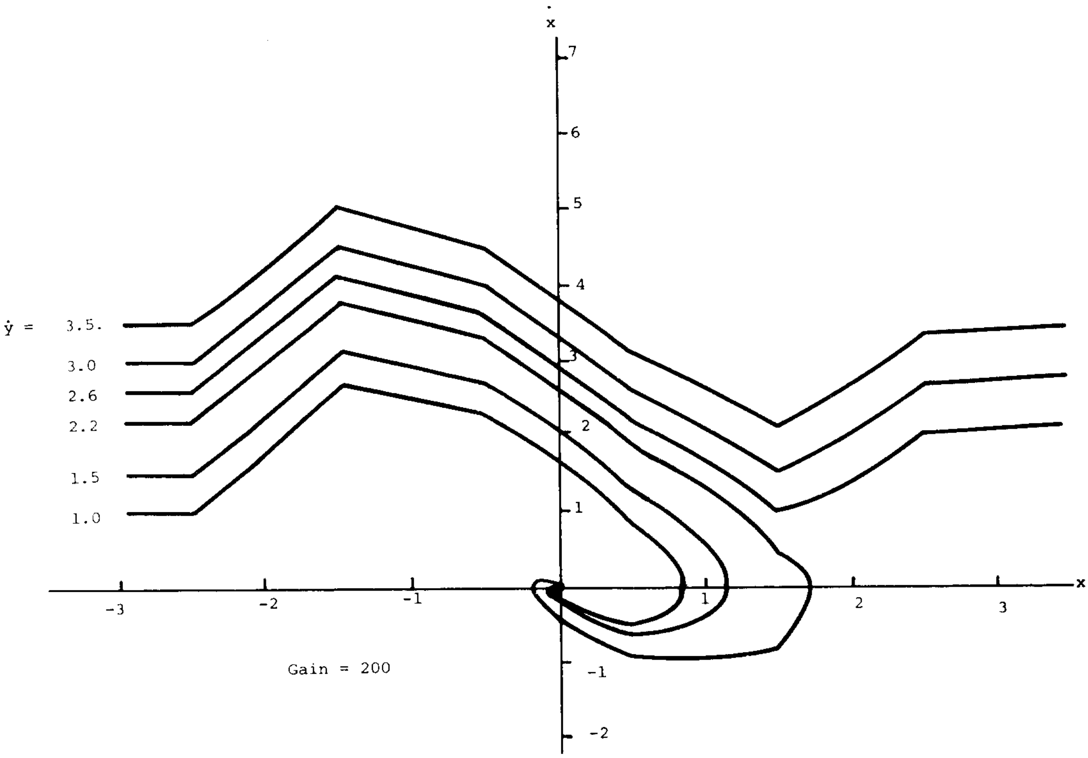

Fig. 5(c). Phase plane plot of 3 - Δ DLL.

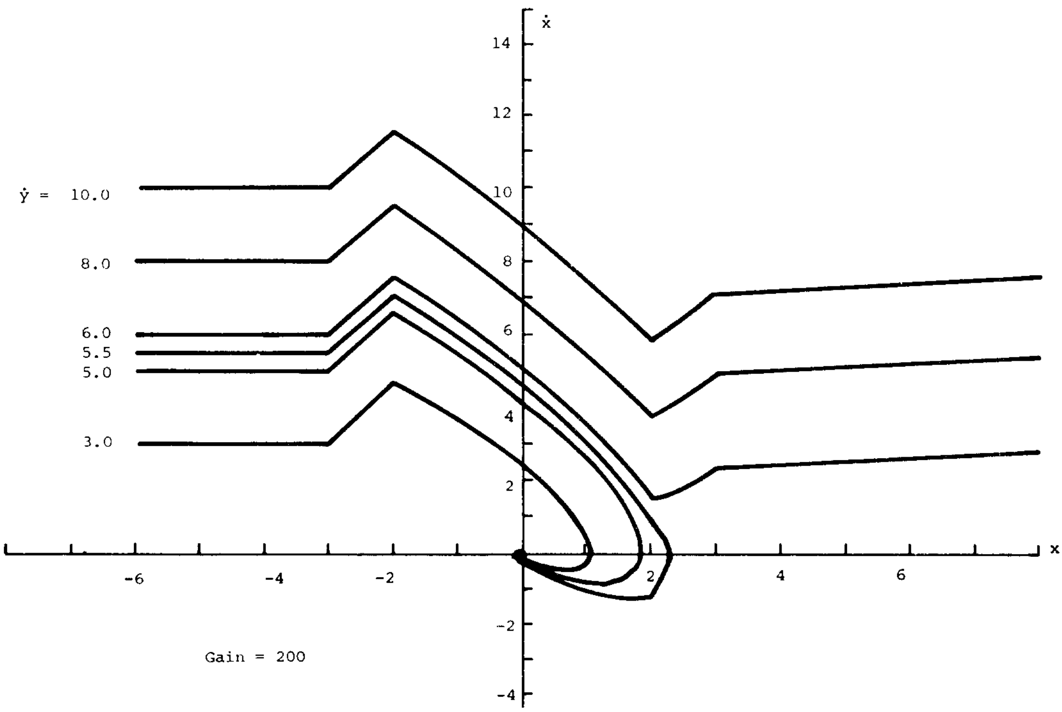

Fig. 5(d). Phase plane plot of 4 - Δ DLL.

where $x = \epsilon/\Delta$, $y = T/\Delta$ and $\dot{x} = \frac{dx}{p_0 dt}$. As examples, we show the plots for 1,2,3, and 4 - Δ DLL's in Fig. 5. The computational step size was in the range of 0.005 to 0.0005. Here the result is exactly the same as that of Nielson [6] for a 2 - Δ DLL, but for 1 - Δ DLL the result is slightly different. Note that the 3 - Δ DLL gets locked on if the normalized input delay differential, $\dot{y}$, is less than or equal to 2.2; otherwise, the DLL becomes out of lock. As for the 4, 5, and 6 - Δ DLL's, the threshold values of $\dot{y}$ are 5.5, 3.3, and 5.9, respectively.

V. Frequency to Lose Lock

We now consider the first passage time of DLL's. Biederman and Holmes derived the first order Fokker-Planck equation for a 1 - Δ DLL, and they obtained from this equation the first passage time [5]. In this section, we generalize this equation for an n - Δ baseband DLL, and compare the results of DLL's with various delays.

The expected time to reach the boundary position for the first time in a conventional PLL was studied by Viterbi [8]. Recall that the system equation of an n - Δ DLL is similar in form to that of a PLL. Therefore, we can obtain the first passage time of an n - Δ DLL directly from Viterbi's result by replacing the PLL parameters with those of DLL. Accordingly, we replace the phase error ϕ with the normalized delay error ϵ/Δ, the input phase θ_1 with the normalized input delay T/Δ, and the signal amplitude with the equivalent input signal amplitude. The DLL boundary positions can be obtained from the correlator characteristic, $D_n(\epsilon)$. Then, the expected first passage time can be expressed as [8]

$$\tau = \frac{1}{\beta} \int_0^{\epsilon_r} d\epsilon \int_{\epsilon}^{\epsilon_r} \exp[\alpha P(x) - \alpha P(\epsilon)]\, dx, \qquad (11)$$

where

$$P(\epsilon) = \int_{-\epsilon_r}^{\epsilon} D_n(x)\, dx,$$

$$\alpha = \frac{4\sqrt{P_s}}{P_d N_o g_o}, \qquad \beta = \frac{P_d N_o g_o^2}{4},$$

and the absorbing boundary ϵ_r determined from the correlator characteristic is $(2n+1)/2$ for an n - Δ DLL.

The frequency to lose locking, F_p, is then obtained by inverting the first passage time. Using the normalized noise bandwidth B_L, and the average

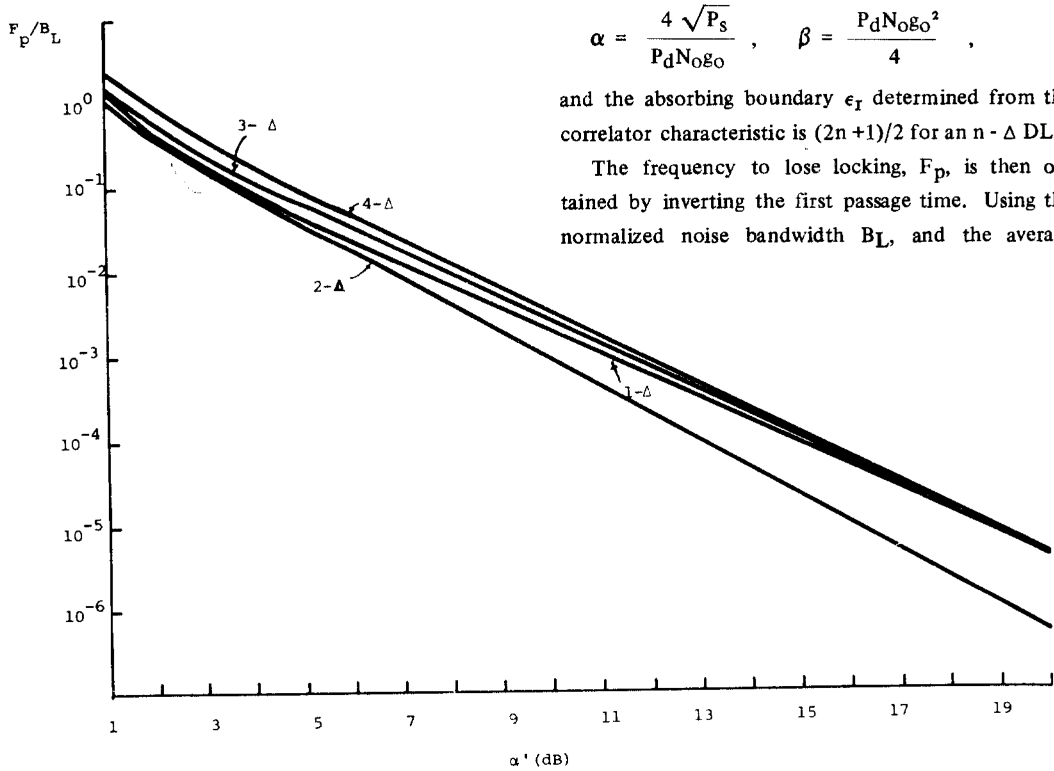

Fig. 6. Frequency to lose lock.

power of combined reference signals P_d, we can write the frequency to lose locking, F_p as

$$F_p/B_L = B/\left\{ \frac{\alpha'}{4P_d} \int_0^{\epsilon_r} d\epsilon \int_{\epsilon}^{\epsilon_r} \exp\left[\frac{\alpha'}{P_d} P(x) - \frac{\alpha'}{P_d} P(\epsilon) \right] dx \right\} \qquad (12)$$

with

$$B_L = \frac{A g_0}{4}, \qquad B = \sqrt{P_s}/A$$

In the above equation α' is the normalized SNR that is equal to αP_d. Note that the coefficient B depends implicitly on the order n of the n - Δ DLL. F_p/B_L is plotted as a function of the normalized SNR α' in Fig. 6. As seen in the figure, the 2 - Δ DLL yields the best performance as far as the frequency to lose locking is concerned.

VI. Conclusion

In this paper we have studied the performance of extended n - Δ DLL's that have advantages in tracking range, noise variance and acquisition over 1 - Δ and 2 - Δ DLL's. For this study we first obtained the system equation of an n - Δ DLL, which turned out to be similar in form to that of a conventional PLL. Using this equation, we obtained the variance of the output noise, and plotted the phase planes of various n - Δ DLL's. In addition, the frequency to lose lock has been considered based on the result of Viterbi. Our study results can be summarized as follows:

(1) With the serial synchronization method, the initial synchronization time of an n - Δ DLL takes only 1/n times that of the 1 - Δ DLL.

(2) In the case of 3 - Δ DLL, its noise variance is three fourth of that of the 2 - Δ DLL in the normal operating range. It gives two times immunity against doppler shift than the 1 - Δ DLL.

(3) As for the frequency to lose lock, the 2 - Δ yields the best performance.

(4) The use of DLL's with delay time greater than 5 - Δ as tracking devices appears to be impractical because of large noise variance.

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