DPLL에 의한 三相誘導電動機의 速度制御 및 安定度에 관한 硏究

論 文
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Speed Control and Stability of 3-Phase Induction Motor with DPLL

朴 旻 鎬* · 玄 東 石**
(Min-Ho Park. Dong-Seok Hyun)

Abstract

The phase-locked loop technique developed in the 1930's has many advantages when applied to speed control.

The speed control and analysis of a three phase induction motor using the PLL are described in this paper. In this system, the phase frequency detector (PFD) compares the actual motor speed from the pulses received from a shaft encoder and desired speed, and the difference adjusts the frequency of the inverter that feeds the motor, and excellent speed regulation in the order of 0.035(%) has been obtained.

A linear continuous model of the drive is developed and system response is analysed using conventional root locus techniques. Various compensating filters and feedback signals are considered and the need for addition of derivative feedback is shown. A sampled data model is used to study the effects of discrete PFD output. Stability limitson speed are predicted. A drive was implimented and experimental results are presented to verify theoretical predictions.

I. Introduction

Phase-locked loops (PLLs) have been used quite successfully in FM receivers, color television, missile tracking, space telemetry, and AM demodulation. Gardner[1] has described much of the history and potential applications of PLLs. Some of these applications date back to the 1930's, when the systems were designed with discrete components. These were, therefore, limited to such cases where better performance would justify the cost of the sophisticated electronic circuitry for the PLL. The situation has changed considerably since then and currently. PLLs are available in the form of a single integrated chip at a very low cost. This has led engineers to find areas of applications of PLLs other than in communications. One such application is the control of the speed of a motor. Volpe[2] has applied the PLL to the control of a synchronous machine. Recently, Moore[3] has presented the fundamentals of applying inexpensive digital integrated-circuit PLLs to the control of motor. Moore has claimed that accuracies of 0.002 percent are possible in speed control. Since this system has fewer components than conventional servosystems, and a much higher accuracy, there are many possible applications. Some examples are conveyor belts, production lines, computer tape drives, and many other situations where the cost, low power, miniature size, and extremely accurate control of speed are important. To be useful in many practical situations, the PLL system should not only have the high accuracy in speed claimed by Moore but should also be able to control the motor over a significant portion of its speed range. Furthermore, it must be capable of main taining lock in the presence of torque disturbances. DC motors have played an important role

* 正會員 : 서울大 工大 電氣工學科 敎授 · 工博
** 正會員 : 漢陽大 工大 電氣工學科 助敎授
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in the speed drive system. However, ac motors such as cage induction motors are robust, rugged, and cheap, With the advance in the solid-state converter, use of induction motors in speed drive system has considerably increased in recent years. This paper presents the development of a variable speed 2-Hp induction motor drive system controlled by a digital PLL feedback network for achieving excellent speed regulation and fast dynamic response, and a study of the stability and dynamic response of such a speed control system The system is first modeled as being linear and continuous, and assessed using con ventional root locus technique. Then consideration is given to the discrete nature of the phase detection output. Finally implementation and experimental results are presented to verify predicted results.

II. Principle of the Phase-Locked Loop

The schematic diagram of the PLL is shown in Fig. 1. The comparator generates a voltage which is proportional to the difference in frequency or phase between the voltage controlled oscillator (VCO) signal ω_0 and the reference oscillator signal ω_i. This error voltage is filtered to produce the required dynamic response and applied to the modulating input of the VCO. The output frequency of the VCO is inversely proportional to its input voltage. If the VCO output is lower in frequency or lags in phase with that of the reference oscillator,the error voltage appearing at the output of the comparator will decrease. The output frequency of the VCO will then increase to compensate for the original error. The error voltage is zero only when the two signals are exactly in phase. The slight lead or lag between the signals will result in a corrective voltage, and compensation will automatically occur. In this way, with a proporly designed filter, the output frequency of the VCO can be made to phase-lock with, and therefore track with extreme precision, the frequency of the reference oscillator. The accuracy with which the VCO output frequency tracks the reference frequency is dependent on the dynamic characteristics of the feedback loop and limited ultimately only by the stability of the reference oscillator.

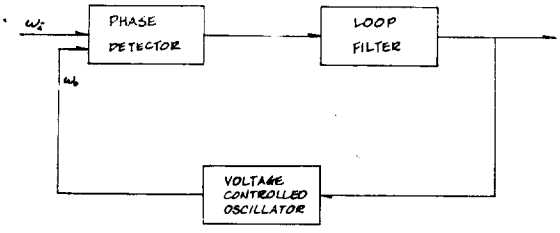

Fig. 1. Schematic diagram of the basic phase-locked loop

III. System Model

Precise speed control of the induction motor drive is achieved by using the PLL technique in a feedback system. The block diagram of such a system which has been studied, analyzed and tested is shown in Fig. 2. In this scheme, instead of comparing the frequency of the VCO with the frequency of the reference oscillator as in Fig. 1, the speed of the motor is compared with the reference frequency. The square wave output of the VCO determines the stator frequency of the induction motor and hence its speed. The transducer is a digital optical encoder whose output frequency is proportional to the motor speed. The output frequency of the transducer automatically tracks the frequency of the reference digital oscillator. If the motor slows down, say due to loading, transducer output frequency will decrease. The detector will generate an error voltage which, after filtering, will increase the output frequency of the VCO. The inverter output frequency will simultaneously increase and compensate for the decreased speed. Similarly, if the motor speeds up, a corrective compensation will decrease the motor speed. The PLL forces the motor speed to synchronize with the reference digital pulse train, thus enabling a precise speed control of the drive. The induction motor is a very robust machine and can be used efficiently for variable speed if a variable frequency supply is available. The improvement in performance obtained by adding slip speed control is well documented.[4]~[7] In addition, flux control provides improvement of performance.[8]~[10] Although such a drive is quite complex, a model which included all such comple-

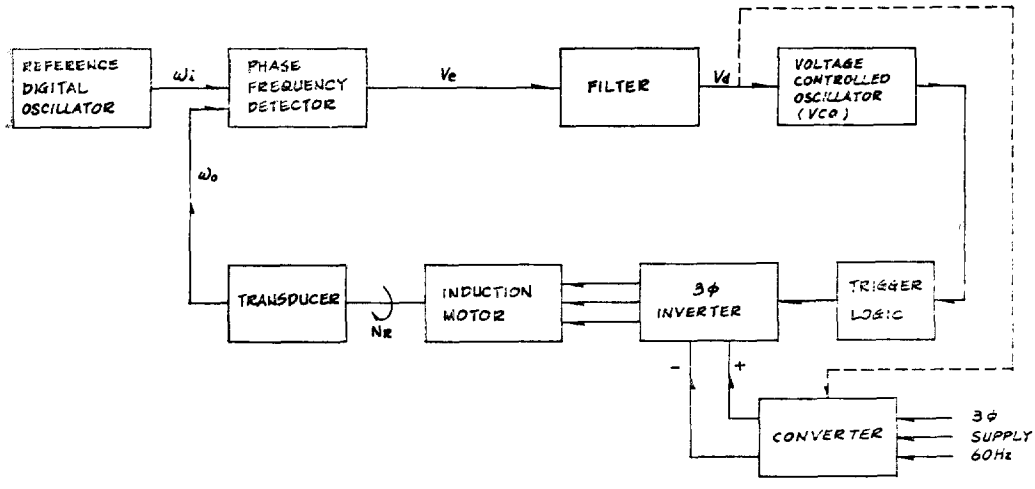

Fig. 2. Block diagram of induction motor drive with PLL

xities would be too cumbersome for assessment of the drive for many different possible controls. It has been shown[11]~[13] that a slip speed controlled induction motor which incorporates flux control can be adequately modeled as a single pole associated with mechanical time constant τ_m and a fixed gain k_m. The output, motor speed, is encoded as a digital pulse train either optically or magnetically sensed. Such an encoder will produce k_0 pulses per shaft revolution, and as such can be modeled as a simple gain. The encoder frequency is fed back and compared to an input reference frequency by the phase detector. The output of the phase detector is proportional to the phase error between the two inputs. Typical waveforms and the average characteristic for a possible detector are shown in Fig. 3. If it is assumed that only the average value of the output is important and that this remains with the bounds ($\pm 2\pi$) of the characteristic, then the phase detector can be modeled as an error detector and a linear integrator (k_d/s). The integral term is due to the fact that the input to the detector are frequency while the output is proportional to phase difference or the integral of frequency error. From Fig. 3, it can be seen that some filtering of the actual phase error signal will be required. Besides, the filter may be used for compensation to improve drive performance. To remain general then, the filter will be described as $F(s)$. The resulting complete system model in order to study the speed regulation. dynamic response, and stability of the system is shown in Fig. 4. The closed loop transfer function can be written as

$$\frac{N_R(s)}{\omega_i(s)} = \frac{G(s)}{1+G(s)H(s)}$$

where

$$G(s) = \frac{k_d F(s) k_m}{s(1+s\tau_m)}$$

$$H(s) = k_0$$

k_m=290r/m/V k_d=2V/rad k_0=32Hz/r/s τ_m=10s

There are certain limits imposed on the different parameters of the model, which will reduce the design flexibility. For example, The mechanical time constant τ_m is fixed by the motor. The gain of the forward path ($G(s)$) has a minimum value because of the desire to control up to a maximum-slip speed and because the phase detector is limited to $\pm 2\pi$. Also a high loop gain is to be avoided because of reduced noise immunity. The gain of the feedback (k_0) has maximum value limited by the physical realizability of the encoder, and a minimum which is determined by the discrete nature of the feedback. This latter aspect is discussed later. It is evident that the performance of the loop will depend considerably on the transfer function of the filter, $F(s)$. One may, like root locus, Bode plots, Nichols charts or other linear control system techniques, to ensure that the loop will be stable as well

as sensitive.

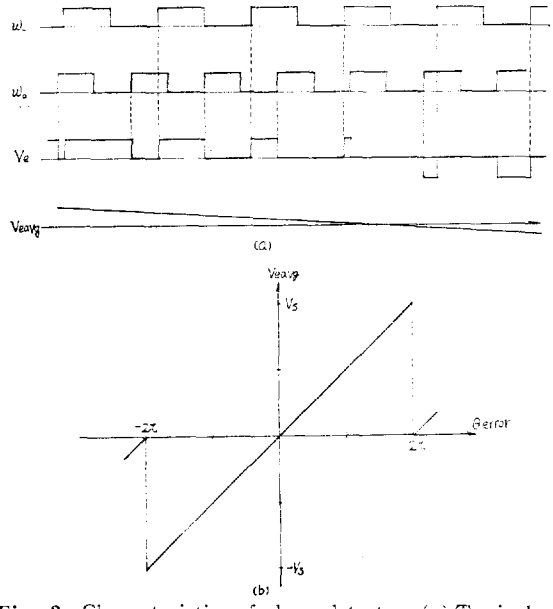

Fig. 3. Characteristics of phase detector. (a) Typical waveforms. (b) Average output characteristic

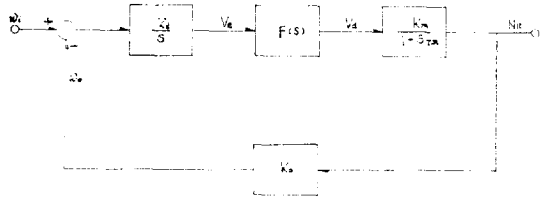

Fig. 4. Transfer function block diagram of induction motor

IV. Root Locus Analysis

Keeping in mind the objective of increased stability and improved pole placement. Root loci are plotted for varying gain and different loop filter transfer functions $F(s)$. While these will be called filters, it is not necessary that the implementation be in the form of the conventional RC-type filter, The first root locus studied is for the case of proportional control or no filter. This is impractical since some filtering is usually required, but it is a good starting point. There are two open loop poles at 0 and $-1/\tau_m$. The root locus for increasing gain is shown in Fig. 5. Becaues of the small real components, as gain is increased, the damping becomes very poor, Any higher order poles which have been neglected, could quickly force the poles into the right-half-plane resulting in stability. Usually some low-pass filtering is required. This adds an open loop pole to the left. In the resulting root locus (Fig. 6) the formerly vertical branches are swept into the right half plane. This indicates unstable operation. An integral term is commonly used in PLL circuits applied in communication systems. This type of filter is shown to be unstable (Fig. 7) for all gains. The addition of a zero which results in proportional-integral phase error control is shown in Fig. 8. This does not improve stability and as such discourages further consideration of any form of integral term. A filter containing both a pole and a zero can have too possible results depending on their relative positions. If the pole is to the right of the zero in the s-plane, the filter is known classically as lag compensation. The root locus, shown in Fig. 9, is not a significant improvement from the low-pass filter case. If the relative pole zero

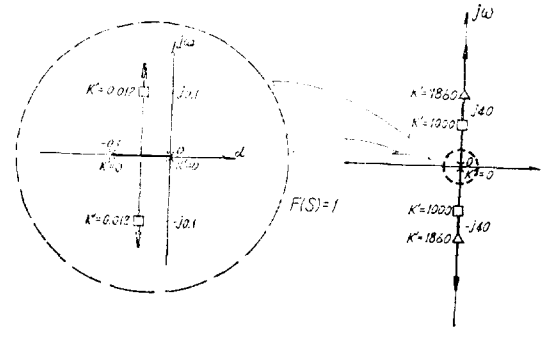

Fig. 5. Root locus plot for phase error control alone with expanded view of origin

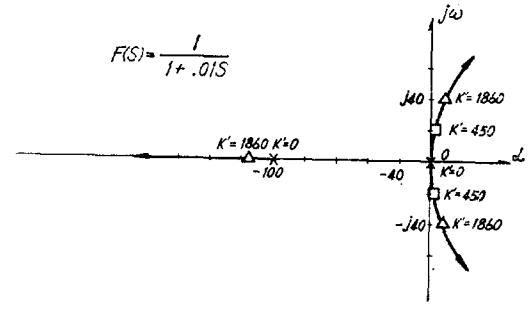

Fig. 6. Root locus plot for phase error control with LP filter

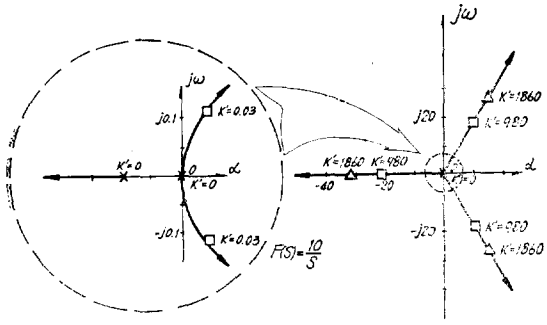

Fig. 7. Root locus plot for phase error integral control with expanded view of origin

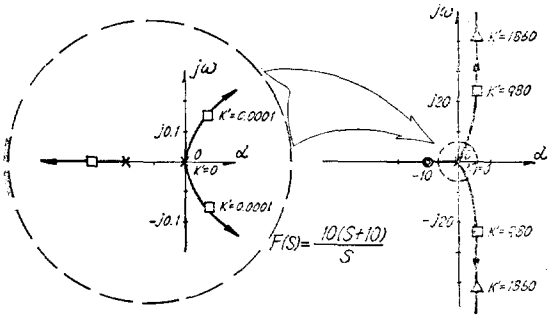

Fig. 8. Root locus plot for proportional-integral control of phase error with expanded view of origin

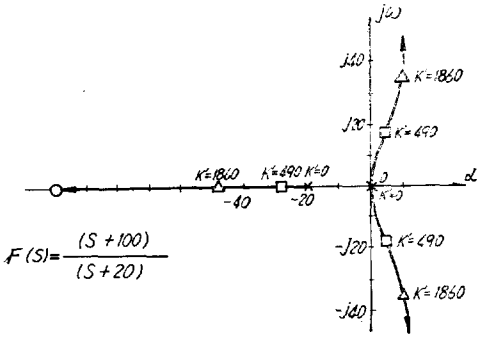

Fig. 9. Root locus plot for lag compensation of phase error control

positions are reversed the filter is known as lead compensation. The corresponding root locus is shown in Fig. 10(a). There is an obvious leftward shift of the dominant poles as the gain increases. This shift becomes more apparent as the open loop zero is brought successively closer to the origin as shown in Fig. 10(b) and (c). Lead compensation results in

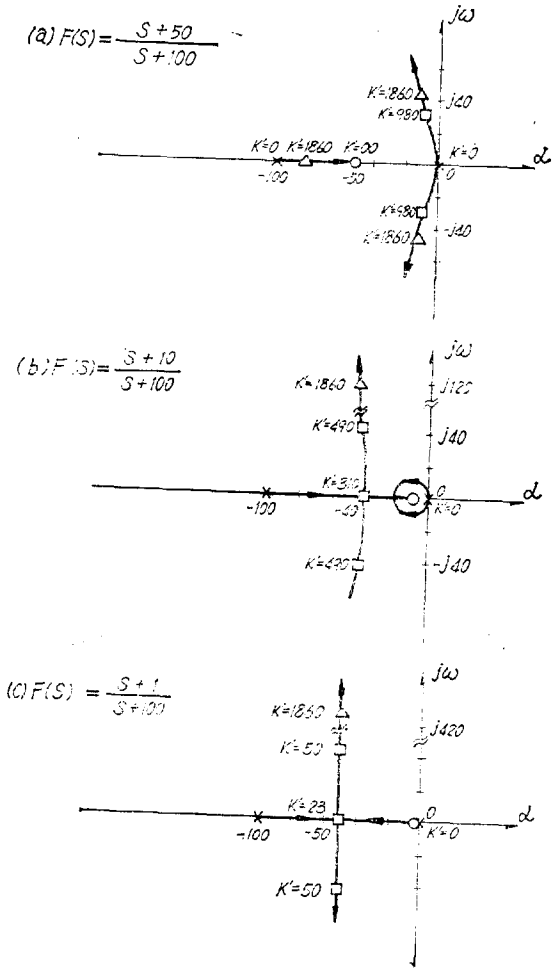

Fig. 10. Root locus plot for lead compensation of phase error control, with zeros at: (a) $s=-50$, (b) $s=-10$, (c) $s=-1$

a differential characteristic over part of the frequency spectrum. From this, one might predict that derivative feedback will be beneficial. Derivative control alone results in a zero at the origin which cancels the pole present there. The result, shown in Fig. 11 is the same as an analog speed control. Phase error control has been eliminated and ZERO SPEED ERROR has been lost. Thus to maintain PHASE LOCK, phase error control must be maintained. The root locus for phase error plus derivative (PD) is shown in Fig. 12. This greatly improves stability. At the same time, the ability to stay PHASE-LOCKED is maintained. It is interesting to note that adding a low-pass filter to the

PD control to reduce high frequency noise response leads to the LEAD COMPENSATION result of Fig. 10(b). Of these many filters, only the lead compensation and PD control cases offer the improvement in stability and response that is desired. These two cases are effectively the same if noise filtering is added to the latter as is usually required.

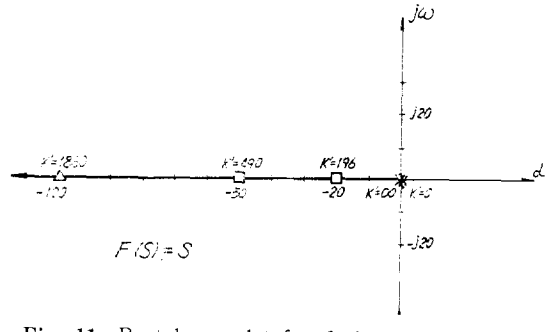

Fig. 11. Root locus plot for derivative control

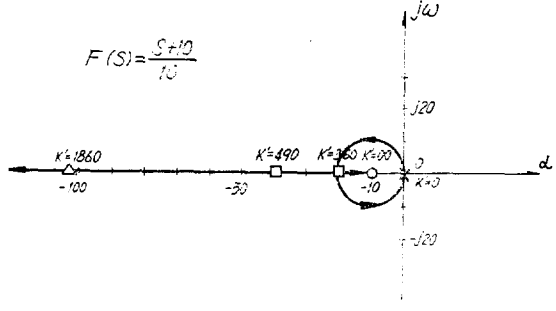

Fig. 12. Root locus plot for proportional plus derivative control

V. Discrete System Analysis

The actual phase detector output can only have discrete voltage levels and the phase error is pulse-width encoded as shown in Fig. 3. In the previous analysis, it was assumed that only the average value was available. Further analys is is therefore required to assess the effect of discrete phase detector output. A linearized sampled data model of the phase detector has been proposed by Tal[14] The transfer function block diagram of the induction motor drive system incorporating the discrete model of phase detector is shown in Fig. 13. Analysis of this discrete model is most easily done in the z domain where root locus methods can again be applied. This involves the z transform which is described in most sampled data control texts[15]~[17] and will not be detailed here. Referring to Fig. 13, the sampling rate T is speed dependent. This complicates an already complex analysis. Thus only the most important case proportional-derivative control will be considered.

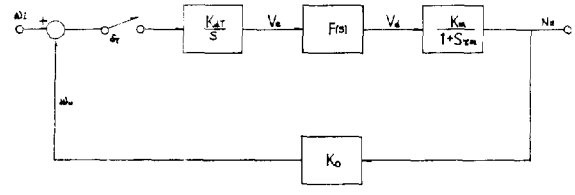

Fig. 13. Transfer function block diagram incorporating discrete model of phase detector $T=2\pi/k_0N_R$

V-I. Proportional Derivative Control

The z transform of $G(s)H(s)$ can be found by performing a partial fraction expansion and looking each term up in a table of z transforms. For the PD case the z-domain open loop transformation will be

$$GH(z)=K'\tau_1 T\frac{z(z-x)}{(z-1)(z-\beta)}$$

where

$$K'=k_0k_dk_m/\tau_m$$
$$x=\tau_m(\beta-1+\tau_1/\tau_m)/\tau_m$$
$$\beta=\exp(T/\tau_m)$$
$$T=2\pi/(k_0N_R)=0.196/N_R$$

The resulting root loci, for certain selected speeds, have been plotted in Fig. 14. Because of familiarity with the s-plane, the z-plane loci are transformed back and plotted again in the s-plane. For the speeds chosen, the discrete system is stable for all gains and is not much different from the continuous case (Fig. 12). If the speed is lowered further, instability may result and it is desirable to define these limits analytically. For continuous systems, such limits are often established using the Routh-Hurwitz criteria. This can also be applied here through use of a second transformation.

$$z=\frac{\omega+1}{\omega-1}$$

This maps the unit circle (stable area) of the z-plane into the left half plane of the complex variable ω. Using this transformation on the open loop transfer function and applying the Routh-Hurwitz criteria, the following constraint results

$$k'\tau_1 T(1+x)+2+2\beta>0$$

It is obviously difficult to evaluate a limit on T in this expression in closed form. For a specific speed, the expression can be solved for the maximum stable gain and such results are presented in Table 1. The minimum speed is seen to be between 6 and 8 r/m for all but low gains. The z-plane loci plots for Fig. 14 may provide an alternative method for obtaining the speed limitations. As long as the zero at x is inside the unit circle, the system will always be stable. From this, the constraint can be written

$$\tau_m(\beta-1+\tau_1/\tau_m)/\tau_1>-1$$

By approximating β by the first two terms of a power series expansion ($\beta=1-T/\tau_m$) and writing

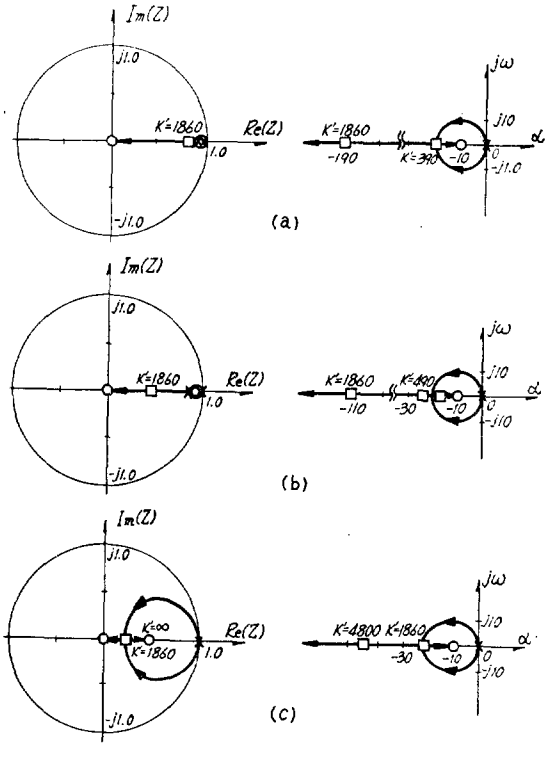

Fig. 14. Root locus plots of proportional-derivative phase error control in both z-and s-plane. (a) 1,100r/m. (b) 120r/m. (c) 50r/m

T in terms of speed N_R, the resulting constraint is

$$N_R>\frac{30}{k_0\tau_1} \text{ r/m}$$

For the typical values used here ($k_0=32$, $\tau_1=0.08$) the lower speed limit is 8.3 r/m. This agrees with results in Table 1.

Table 1. Stability limit of gain for proportional-derivative control

speed(rpm)	maximum stable gain
1	2
2	6
3	17
4	42
5	89
6	190
7	453
8	3012
9	NO LIMIT
10	NO LIMIT

Table 2. Stability limit of gain for proportional-derivative control with zero order hold

speed(rpm)	maximum stable gain
20	236
40	457
60	704
80	932
100	9110
120	1400
140	1655
160	1897
180	2016
200	2234

V-II. Zeroth Order Hold

In a practical system it is often undesirable to apply a pulse train to the continuous system. For this reason, holding circuits are used[15]-[18] to reconstruct a signal. The purpose of these are to maintain the sampled value or a function of it during the following period. This is typical of computer control systems. The effects of the addition of such a holding circuit is investigated. The most common implementation, zeroth-order hold, is shown in Fig.

15 in which the sampled value is maintained for one period. The impulse response of such a circuit is

$$g(t)\begin{cases} 1/T, & 0<t<T \\ 0 & \text{elsewhere} \end{cases}$$

The Laplace and z-transform of this are

$$G(s)=\frac{1-e^{-Ts}}{Ts}$$

$$G(z)=\frac{(z-1)z}{z}\left(\frac{1}{Ts}\right)=\frac{1}{T}$$

The PLL system can be analyzed in the z domain including the zeroth-order hold. The overall z transfer function for the proportional-derivative control case will be

$$GH(z)=k'\tau_m\frac{(\tau_m-\tau_1)(-1+T/(\tau_m-\tau_1))(z-x)}{(z-1)(z-\beta)}$$

where

$$x=\frac{(1+T/(\tau_m-\tau_1))-1}{\beta+T/(\tau_m-\tau_1)-1}$$

The gain, the zero, and one of the poles are speed dependent. The resulting z-plane and s-plane root loci are plotted in Fig. 16. As the speed increases, the s-plane loci approach those of the continuous case for low gains (Fig. 12) as expected. For any

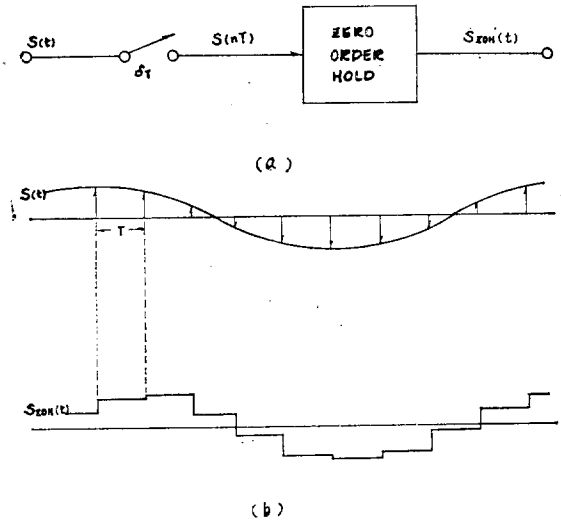

Fig. 15. Zeroth-order hold circuit. (a) Block diagram. (b) Waveforms

speed there is a maximum stable gain or conversely for a gaven gain there will be a minimum stable speed. Such limits can be defined using the previous method. Two constraints result

$$1-\beta+k'\tau_m(\tau_m-\tau_1)(\beta(1+T/\tau_m-\tau_1))-1)>0$$

and

$$2+2\beta-k'\tau_m(\tau_m-\tau_1)(T/\tau_m+\beta(2+T/(\tau_m-\tau_1))-2>0$$

Again it is difficult to define the limits in closed form, but for a given speed a maximum stable gain can be computed. These computer results are shown in Table 2. An approximate closed form solution relating gain and speed at the point of first instability can be obtained by referring to the root loci of Fig. 16. The z-domain root loci are described by the equation

$$z^2+(k_z-1-\beta)z+(\beta-k_z x)=0$$

where

$$k_z=k'\tau_m(\tau_m-\tau_1)(\beta-1+T/(\tau_m-\tau_1))$$

Instability first occurs at $z=-1$. Making the approximation that $1+\beta=2$ and taking $x=1$ as the worst case, the gain limit is

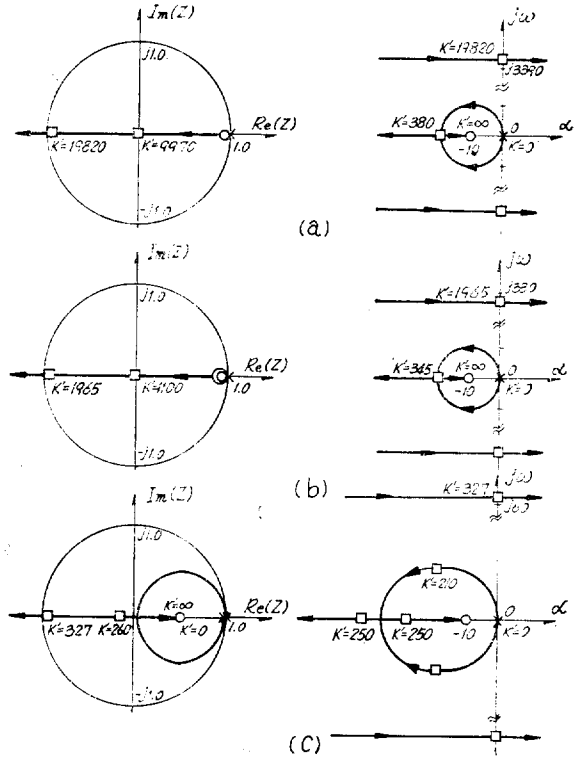

Fig. 16. Root locus plots of proportional-derivative phase error control with zeroth order hold. (a) 1,100r/m. (b) 120r/m. (c) 50r/m

$k_z<2$

Approximating β and simplifying as before, the limit becomes

$$N_R>\frac{30\tau_1 k'}{k_0}$$

This agrees with the results in Table 2. For the typical values used ($k'=1860$, $k_0=32$, $\tau_1=0.08$), the minimum speed is 180 r/m. In general, the discrete phase detector output will cause a lower limit on speed for stable operation. This lower speed limit may not be of practical importance if the drive does not require operation at this low speed.

VI. Experimental Results

The system is built and tested using a 2-Hp induction motor with the various filters. The frequency of oscillation is found to be in 1~3Hz range depending on the load. Over the tested range of speed, the maximum oscillation encountered was 0.25 percent of the operating speed. The various filters discussed earlier were implemented and the phase error and speed responses recorded in Fig. 17 and Fig. 18, respectively. Referring to these two figures, the cases of phase error alone (a) and phase error low pass filtered, (b) are both stable but slightly oscillatory. This was predicted earlier. Also as predicted, the two cases involving integral term, (c) and (d) are both unstable. Note that the phase error rises to 2π repeatedly. As the phase error increases further, the recorded value drops to zero and rises again. This indicates a large variation in phase and a LOSS OF LOCK by the PLL.

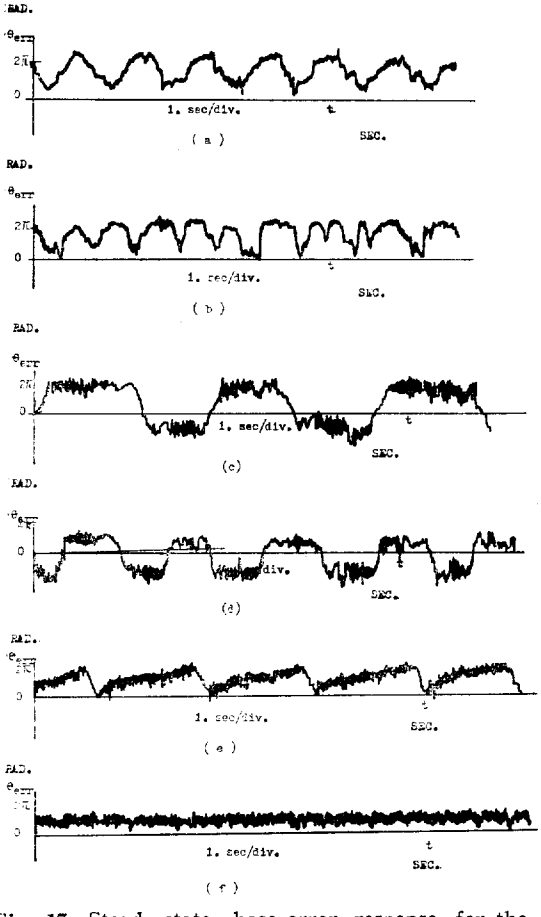

Fig. 17. Steady-state phase error response, for the following controls; (a) PPE. (b) FPE. (c) ITL. (d) PI. (e) DO. (f) P&D

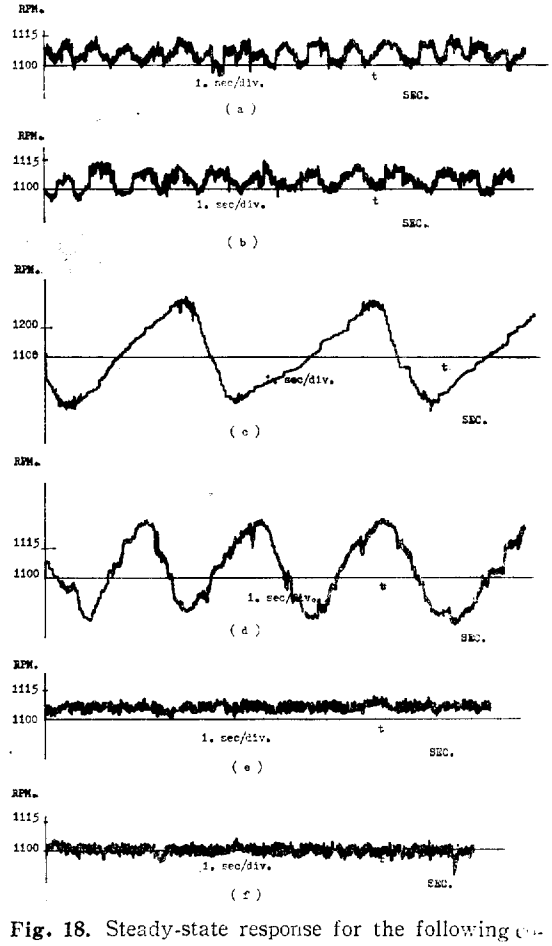

Fig. 18. Steady-state response for the following controls; (a) PPE. (b) FPE. (c) ITL. (d) PI. (e) DO. (f) P&D

Thr use of frequency error alone is quite stable with respect to speed as shown in Fig. 18(c). However, a steady-state speed error is present and the phase error ramps form 0 to 2π as seen in Fig. 17 (c). This indicates a loss of lock. The combination of phase error and frequency error or proportional derivative control is shown in Fig. 17(f) and 18(f). This case is quite stable with respect to both phase and frequency. Tests are performed to obtain torque-speed characteristics under constant voltage and constant volt/hertz mode of operation of the induction motor. The results are shown in Figs. 19 and 20, respectively. As expected from the theory of induction motor, drooping torque-speed characteristics are obtained with constant voltage operation and essentially constant torque characteristics are obtained for the constant volt/hertz operation.

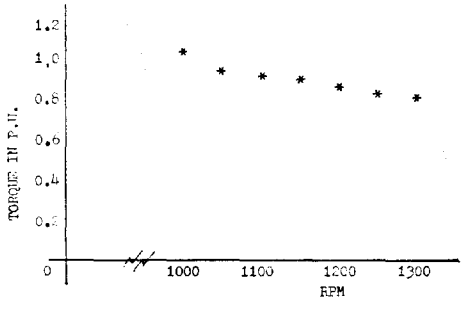

Fig. 19. Torque speed characteristic at constant stator voltage

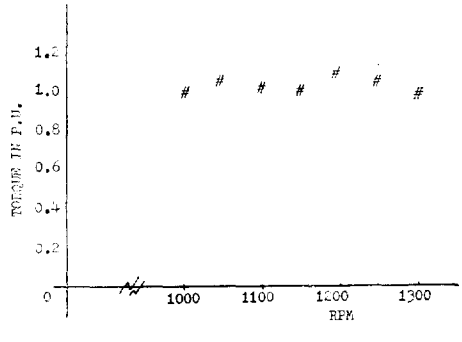

Fig. 20. Torque speed characteristic at closed-loop consrant volt/hertz operation

VII. Conclusion

The feasibility of using digital PLL in induction motor drive is demonstrated. Precise speed regulation is achieved. The system has the ability to recover from loss of lock, which can be caused by a large disturbance. The motor speed is insensitive to the normal changes in the power supply and frequency. Assessment of a linear continuous model showned that the addition of derivative feedback is required for stable operation and the desired dynamic response. It has been found that the phase error derivative could be provided adequately by using frequency error feedback, without a degradation in noise immunity. Consideration of the discrete phase detector output shows a lower speed limit for stable operation. However, this limit may not be of importance because of frequency limitations imposed by the inverter. The mathematical model developed and studied qualitatively is an important tool in predicting the system behavior. A more rigorous model with both qualitative study will reveal more insight into the system performance. The consideration of the nonlinearities in the system could be incorporated in the model. Simulation is another tool which could help in a better understanding of the system. The system studied in this paper combines the excellent speed regulation characteristics of the PLL with the numerous advantages of the induction motor over the dc motor. It has great potential as a speed drive system.

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