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A Two Dimensional Analysis of the Low Level Currents in Buried Channel MOS Trasistors (Buried Channel MOS Transistor에서의 미소 전류에 대한 2차원적 해석)

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要 約

Buried Channel MOS 트랜지스터에서의 미소전류(Subthreshold Current)를 2차원 평면에서 Poisson 방정식과 연속 방정식을 Interactive 하게 적용함으로써 계산하였다. 계산 결과를 실험 결과와 비교하였고 미소 전류 영역에서는 두 결과가 비교적 잘 일치하고 있음을 보였다.

Abstract

Low level currents in a buried channel MOS transistor have been computed numerically by solving the Poisson's equation and continuity equation in a two-dimensional space. The results are compared with experimental measurements in terms of the drain current. Reasonable agreement has been found in the subthreshold region where the drain current depends on the gate-to-source voltage exponentially.

Introduction

With the advancement of the buried channel charge coupled device (CCD)[1,2,3] technology, interests on the buried channel MOS transistor or Junction and Insulated Gate Field-Effect Transistor (JIGFET)[4] have grown considerably recently. This is mostly due to the fact that a buried channel MOS transistor is a natural MOS transistor to be fabricated on the same chip with a buried channel CCD using an identical processing sequence. Besides the processing compatibility, the buried channel MOS transistor has higher transconductance, better linearity, and lower noise when compared with a conventional surface channel MOS transistor[4] The low noise property of the buried channel MOS transistor is often utilized in the charge detection scheme of a CCD such as floating gate amplifier (FGA)[5], and distributed floating gate amplifier (DFGA)[6]. Theoretical analysis of DFGA noise[7] shows that the signal-to-noise ratio of the amplifier has the maximum value when the buried channel MOS transistor is biased near the boundary of the subthreshold region.

Although the buried channel MOS transistor is widely used in practice for the charge detection scheme in a buried channel CCD, theoretical analysis of the transistor in and near the subthreshold region has not been carried out in sufficient detail. Barron[8] has given analytic expressions of the subthreshold current for the conventional MOS transistors. This model, however, is not adequate for a burried channel MOS transistor where the drain current is confined in a region which is always kept away from the silicon/silicon dioxide interface.

Masuhara and Etoh[9] calculated the surface electron density in the subthreshold region of implanted MOS transistors, but could not attain

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drain current characteristics therefrom. This is due to the fact that, with some drain-to-source bias voltage applied, there exists a great asymmetry in the electron concentration and potential distribution along the channel, which necessitates the use of a two-dimensional analysis.

This paper reports the results of a two-dimensional calculation of the drain current of a buried channel MOS transistor. Both the subthreshold region and the normal operating region are treated in a unified manner without resorting to curve fitting methods. The numerical method developed for JFET[10] has been used with appropriate modifications.

Device Model and Results

The cross-sectional view of the buried-channel MOS transistor is shown in Fig.1. The n-region underneath the gate oxide is formed by ion-implantation resulting in a Gaussian impurity profile. In the normal operating bias range, there

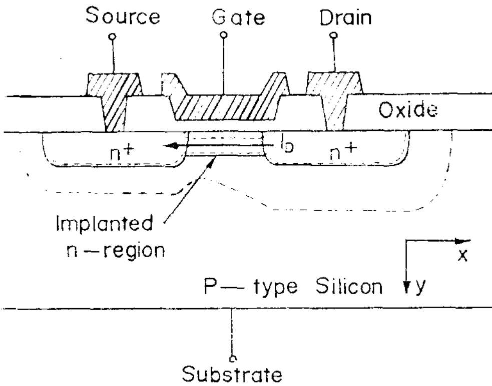

Fig.1. Cross-sectional view of a buried channel MOS transistor.

exists depletion regions both at the silicon/silicon-dioxide interface and n/p junction formed by the implanted region and the substrate. The drain current, therefore, is confined within the implanted n-region and is alway kept away from the interface. Since the drain current is flowing inside the bulk region, the bulk mobility determines the current rather than the surface mobility, thereby giving higher transconductance. The $1/f$ noise of conventional MOS transistor is also suppressed because the electrons for the drain current is not interacting with the surface states. In the subthreshold region, the number of electrons in the conductive channel between the source and drain decreases, and the drain current is determined by the electro static potential and electron distribution near the source region.[10]

In general, the drain current is obtained by

$$I_D = Z\int q\mu_n \, n\frac{\partial \varphi_n}{\partial x} \, dy \cdots\cdots \text{Equ.1}$$

where Z is the channel width perpendicular to the figure, μ_n is the bulk mobility and φ_n is the quasi-Fermi level for electrons. Since the electron density, n, is related to the electro-static potential, ψ, as

$$n = n_i \exp\left[\frac{q(\psi-\varphi_n)}{kT}\right] \cdots\cdots \text{Equ.2}$$

one can compute the drain current from $\psi(x,y)$ and $\varphi_n(x,y)$. The electrostatic potential and the quasi-Fermi level for electrons are obtained by solving the Poisson's equation and the continuity equation simultaneously. These are

$$\nabla^2\psi = \frac{-q}{\epsilon_s\epsilon_0}[N_D - N_A - n + p] \cdots\cdots \text{Equ.3}$$

$$\nabla\cdot J_n = -\nabla\cdot[q\mu_n\cdot n\cdot\nabla\varphi_n] = 0 \cdots\cdots \text{Equ.4}$$

Note that the net rate of recombination has been taken to be zero in Equ.4. This is a reasonable approximation for the device since most of the drain current is due to the majority carriers, i.e., electrons inside the channel.

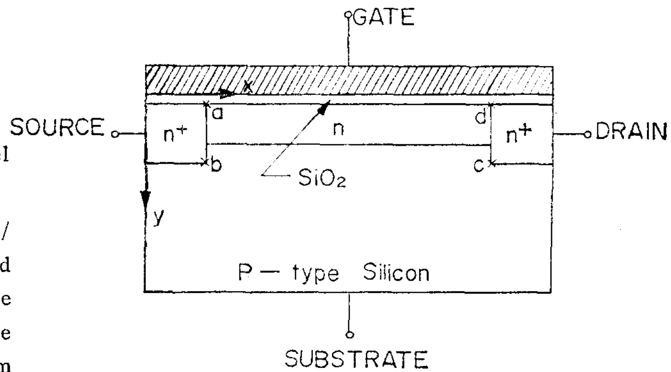

Fig.2. Device model for the two-dimensional numerical calcultion.

Both Equ. 3 and 4 have been solved for a simplified device model shown in Fig.2, by using

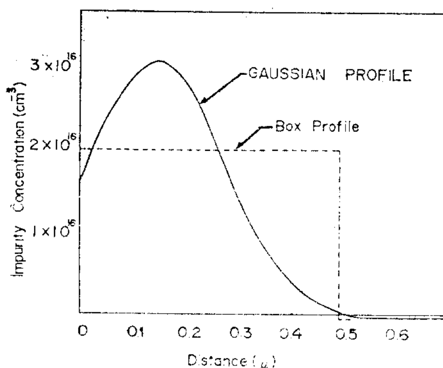

Fig.3. Gaussian impurity profile resulting from ion-implantation and box-profile approximation.

numerical technique reported in Ref. 10) with appropriate modifications. The doping profile of the implanted n-layer has been approximated by a box-profile as shown in Fig.3. The impurity concentration and the junction depth of the box-pro file have been chosen in such a way that the channel location remains the same as for the Gaussian profile. This approximation results in a slight increase (about 10%) for the total number of impurities in the implanted layer. However, as will be shown later, the more serious problem in this approximation is that it

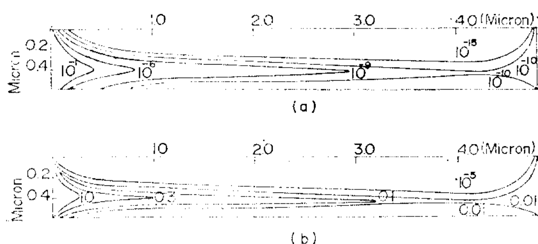

Fig.4. Distribution of electron concentration in side the rectangular region a-b-c-d of Fig.2. The electron concentration is normalized by the doping level of the n-region ($2\times10^{16}cm^{-3}$).
$V_G=5$ Volts, $V_D=14$Volts, $V_{SUB}=0$ Volt and $V_S=9$ Volts for (a), $V_S=8$ Volts for (b)
Flat band voltage is taken to be zero.
oxide thickness=0.12 micron
channel length=5 microns

has resulted about five-to-ten times increase of the impurity concentration at the channel location, i.e., about 0.4μm deep from under the gate oxide. The results of two-dimensional computation is shown in Fig.4 for the sub-threshold region and normal operating region in terms of electron concentration. The formation of the conductive channel inside the bulk n-region and channel pinch-off near the drain is clearly observed in the normal operating region. In the subthreshold region, most of the implanted region is depleted except very near the source region. In this case, the drain current is believed to be due to the electrons that are injected from the source n^+ region to the channel region.

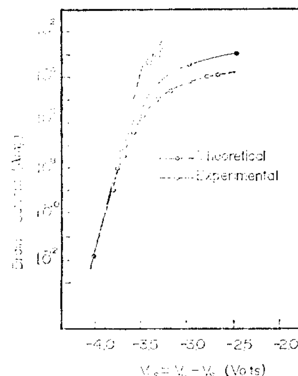

Fig.5. Drain current vs. gate-to-source voltage $V_S=7.5\sim9$Volts, $V_D=14$ Volts, $V_G=5$ Volts with substrate grounded.

The results of the numerical computation have been compared with the experimental data in terms of the drain current in Fig.5. The experiment has been carried out on the test MOS transistor in Fairchild CCD 110 chip using three independent voltage sources for the bias of the drain, the gate, and the substrate terminals, while grounding the source. The drain current is measured with Keithley 610 C Electrometer while varying the source-to-substrate voltage and keeping the other bias voltages constant. The circuit diagram of the experimental set-up is shown in Fig.6.

The experimental curve shown in Fig.5 has been matched with the theoretical one by shifting the former horizontally by 1.68 Volts to take

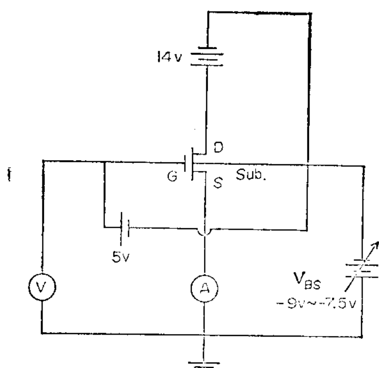

Fig.6. Measurement Circuit.
A : Keithley 610C Electrometer
V : Keithly 616 Digital Electrometer

care of the non-zero flat-band voltage. The agreement between the numerical result and the experimental measurement is reasonable in the subthreshold region where the drain current depends exponentially on the gate-to-source voltage. This indicates the validity of the numerical method employed in the subthreshold region. As can be noticed in Fig.5, however, comparatively large discrepancy exists between the two curves in high and medium current levels. This discrepancy is believed to be partly due to the series resistances of the source and the drain region and partly due to the box-profile approximation which resulted in about five-to-ten times increase of the impurity concentration at the channel location, thereby increasing the channel conductance for the medium and high current levels.

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