새로운 高周波用 MOS 트랜지스터의 試作에 관한 硏究

論 文
27～4～2

Study on Experimental Fabrication of a New MOS Transistor for High Speed Device

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Abstract

A new method of realizing the field effect transistor with a sub-μ channel width is described. The sub-μ channel width is made possible by etching grooves into $n^+ pn^- n^-$ structure and using p region at the wall for the channel region of the Metal-Oxide-Semiconductor transistor (MOST), or by diffusing two different types of impurities through the same diffusion mask and using p region at the surface for the channel region of MOST.

When the drain voltage is increased at the pn^- drainjunction the depletion layer extends into the n^- region instead of into p region; this is also the secret of success to realize the sub-μ channel width.

As the result of the experimental fabrication, a microwave MOST was obtained. The cut-off frequency was calculated to be 15.4 GHz by Linvill's power equation using the measured capacitances and transconductance.

I Introduction

Field effect transistors (FET) have potentially high speed capability. The devices obtainable until now, however, have not sub-μ passed the frequency limitation of bipolar devices.

The main barriers against the realization of high speed devices are summarized as follows.

1) The sub-μ channel length is not obtained because of the geometrical limitation due to the photo-engraving technique.
2) Even if sub-μ channel is realized, the FET action is obstructed by the limitation of the electical characteristics, one example of which is the output conductance.
3) The parasitic capacitance to the intrinsic capacitance ratio increases as the channel length decreases.

A great deal of effort has been made to overcome these limitation, for instances, electron beam processing[1] for the fine pattern, gate-drain self alignment process[2] for small parasitic capacitance, tetrode construction[3] for the reduction of the feedback capacitance. These efforts also encounter the limitation of the electrical characteristics such as the increase of the output conductance due to the effective channel length modulation by the depletion layer widening.

We propose a new device construction by which the sub-μ channel length is easily realized by today's photoengraving technique and the limitation

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of the electrial characteristics is solved.

The channel length is determined by the distance between diffusion fronts of double diffused semiconductor regions. The electric characteristics of this high speed sub-μ MOST show low output conductance, high drain breakdown and effectively no punch through current.

II. Basictheory

1. Theory of MOS transistor.

The basic structure of the insulated gate device is illustrated in Fig.1.

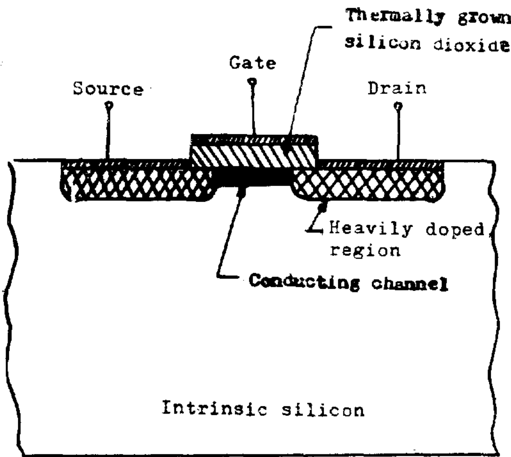


Fig. 1. Insulated-gate field effect transistor.

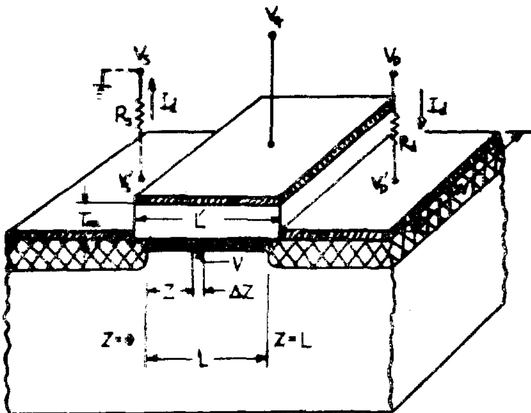


Fig. 2. Schematic representation used in calculations.

The channel, source and drain contacts and control electrode are fabricated using conventional diffusion photo resist, and vacuum evaporation techniques.

With reference to Fig.2, let the drain current be I_d, with the external source connection grounded and with the external drain and gate electrodes biased at V_D and V_G, respectively. The internal source and drain connections differ in potential from the accessible terminals by the potential drop across the parasitic series resistances R_S and R_D, respectively.

An electron conduction device is considered, and n^+ source and drain contacts are employed. The potential at some point Z in the channel is given by $V(Z)$, where $0 \leq V(Z) \leq V_D$.

With a thick oxide implicitly assumed, one has

$$E_{ox}(Z)=\frac{V_G-V(Z)}{T_{ox}} \qquad (1)$$

and $$\sigma_c(Z)=\varepsilon_{ox}E_{ox}(Z)=\frac{\varepsilon_{ox}}{T_{ox}}[V_G-V(Z)] \qquad (2)$$

where σ_c is the induced surface-charge density in the channel at point Z, δ_{ox} is the dielectric constant of the oxide and T_{ox} is the oxide thickness. By the definition of V_p (V_p is the pinch -off voltage) there will be mobile charge at the point Z, only if

$$V_G-V(Z)\geq V_p$$

Thus we have for the mobile charge density σ_m at any point[7]

$$\sigma_m(Z)=\frac{\varepsilon_{ox}}{T_{ox}}\{[V_G-V(Z)]-V_p\}, \quad \text{for } V_G-V(Z)>V_p$$

$$\sigma_m(Z)=0, \text{ for } V_G-V(Z)\leq V_p \qquad (3)$$

The conductance $G(Z)$ of the infinitesimal channel section of width W and of length ΔZ is given by

$$G(Z)=\frac{\sigma_m(Z)\mu W}{\Delta Z} \qquad (4)$$

where μ is the carrier mobility[8] ohm's law yields the drain current

$$I_d=G(Z)\Delta V=\sigma_m(Z)\mu W\frac{\Delta V}{\Delta Z} \qquad (5)$$

hence

$$I_d=\frac{\varepsilon_{ox}\mu W}{T_{ox}}[V_G-V_P-V(Z)]\frac{\Delta V}{\Delta Z} \qquad (6)$$

An integration from one end of the channel to the other yields

$$I_d\int_0^L dz=\frac{\varepsilon_{ox}\mu W}{T_{ox}}\int_{V_S'}^{V_D'}[V_G-V(Z)-V_P]dV \qquad (7)$$

$$I_d=\frac{\varepsilon_{ox}\mu W}{LT_{ox}}\left\{(V_G-V_P)(V_D'-V_S')-\frac{1}{2}(V_D'^2-V_S'^2)\right\} \qquad (8)$$

The two auxiliary equation needed to eleminate V_D' and V_S' are

$$V_D'=V_D-I_dR_D,\quad V_S'=I_dR_S \tag{9}$$

and substitution into(8) yields the desired set of drain characteristics for this device. However, this solution is valid only for $V_G-V_D'\geq V_P$, for when the difference between gate and internal drain voltage is less than V_P, the channel is pinched off near the drain and the limits of integration used in (7) are no longer valid.

As in the Shockley unit, the current remains essentially constant [1] for larger valuesof drain voltage and will be designated by I_{ds} Imposing the condition that $V_D'=V_G-V_P$ yields Ids from (8) and (9) :

$$I_{ds}=\beta\frac{(V_G-V_P)^2}{1+\beta R_S(V_G-V_P)+\sqrt{1+2\beta R_S(V_G-V_P)}} \tag{10}$$

and

$$\beta\equiv\varepsilon_{ox}\mu W/LT_{ox} \tag{11}$$

It should be noted that for small values of series source resistance the transfer function is essentially parabolic yielding a square law device. The drain current beyond saturation is essentally independent of the parasitic series drain resistance R_D. This resistance merely increases the drain voltage at which the drain current saturates.

Differentiating (10) yields the transconductance (g_m) of the device as shown below,

$$g_m=\frac{\partial I_{ds}}{\partial V_G}$$

$$=(2\beta)\left(\frac{(V_G-V_P)}{1+2\beta R_S(V_G-V_P)+\sqrt{1+2\beta R_S(V_G-V_P)}}\right) \tag{12}$$

The total input capacitance C_{in} is simply the parallel plate capacitor formed by the gate electrode of area $L'W$ separated from the semiconductor by spacing T_{ox}. In practice, $L'\gtrsim L$ and the g_m/C_{in} ratio is a good measure of the frequency response of this device.

$$g_m/C_{in}=\left(\frac{2\mu}{L^2}\right)\left(\frac{(V_G-V_P)}{1+2\beta R_S(V_G-V_P)+\sqrt{1+2\beta R_S(V_G-V_P)}}\right) \tag{13}$$

And the frequency characteristics of the power gain is described by the channel cut-off frequency and the feedback capacitance cut off frequency.

2. Diffusion self-alignment for sub-μ channel in DSA MOST

In the conventional MOST, the most important dimension, the channel length is destermined by the photo-engraved planar geometry. In the proposed new MOST the channel length is determined by the double diffused semiconductor region.

One method of realizing the double diffused layer is to etch the groove as deep as the drain junction to be and grow a gate oxide. Fig. 3. shows a schematic cross-section of this structure.

The gate electorde overlaps over the source region through the thin gate oxide only by sub-μ distance, and the other part of the gate electrode is laid on the thick oxide.

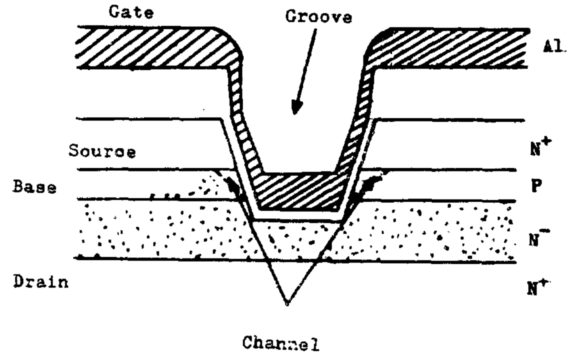
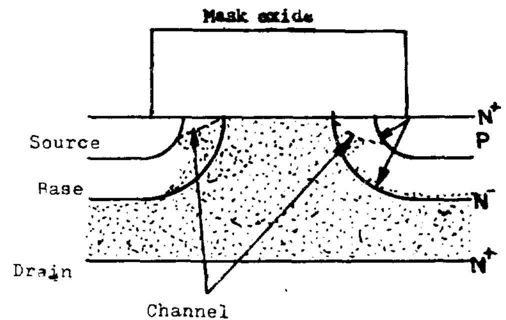


Fig. 3. Cross-section of the diffusion self-aligned MOST (DSA MOST) -non planar type-

So the drain-gate feedback capacitance is reduced by making the planar geometry of the etched groove slim and designing the thick depletion layer to exist under the gate electrode. Another method is to use the same diffusion mask in the double diffusion as shown in Fig.4.



* Self alignment by diffusion

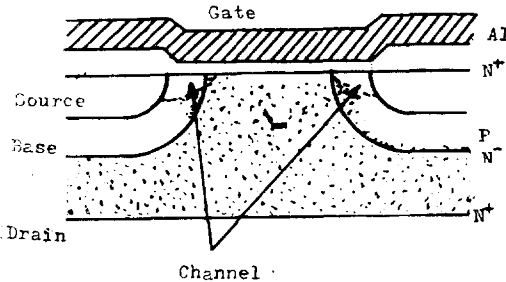


Fig. 4. Cross-section of DSA MOST -planar type- (top) with the diffusion mask, (bottom) with the gate electrode.

The drain-gate feedback capacitance is reduced by employing a surrounding sources structure and widen the depletion layer over the whole surface of the surrounded drain region.

A little disavantage of the planar structure, however, is that carrier must travel the longer n^- layer to reach the n^+ substrate, which somewhat degrades high-frequency preformance.

As is described above, the channel length is not limited by the accuracy of photo-engraving technique and the channel is selfaligned by double diffusion. We call these MOST's as diffusion selfaligned MOST's; the former type as non-planar type and the latter type as planar type. The both types promise the realization of GHz MOST's.

3. Design principle

The equivalent circuit of MOST is shown in Fig. 5. If the parasitic resistances are negligibly small, the conjugately matched power gain caculated from Linvill's relation[4] is given as

$$P_{out}/P_{input}=\{[1/1+(\omega/\omega_c)^2]^2+(\omega/\omega_c)^2 [1/1+(\omega/\omega_c)^2+\omega_c/\omega_r]^2\}/ \{4nr/1+(\omega_c/\omega)^2+2[1/1+(\omega/\omega_c)^2+\omega_c/\omega_r]\omega_c/\omega_r(\omega/\omega_c)^2\}$$

where,

$$\omega_c=(r_cC_{GC})^{-1},\quad \omega_r=g_m/C_{GD},\quad n=(r_cg_m)^{-1},$$
$$r=(r_{ds}g_m)^{-1}$$

r_c : Channel resistance.

r_{ds} : drain to source resistance.

C_{GC} : gate-channel capacitance

C_{DG} : gate-drain capacitance

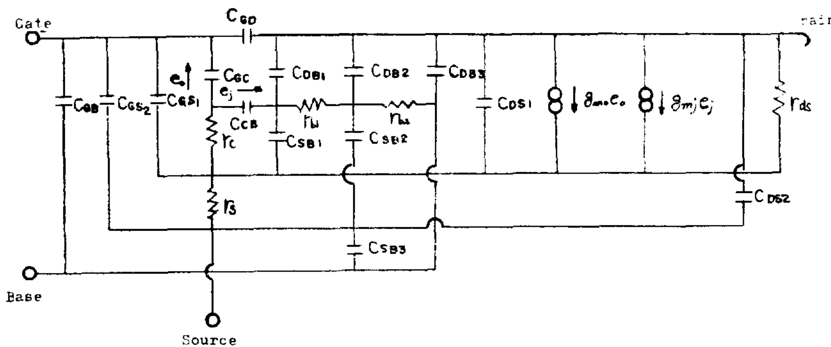


Fig. 5. Equivalent circuit of DSA MOST

Thus, the frequency characteristics of the power gain is described by two cut-off frequencies, which are the channel cut off frequency $f_c=\frac{\omega_c}{2\pi}$ and the feed back capacitance cut-off frequency $f_r=\frac{\omega_r}{2\pi}$ To design a high frequency MOST, both frequencies must be made as high as possible.

The relation between r_c and g_m is reported experimentally[5] and theoretically[6]. There are various cases ranging from $n=1$ to $n=9$. Here we esimate $1/\omega_c$ as roughly a half of the channel transit time, that is $\omega_c \gtrsim 2g_m/C_{GC}$. In the carrier velocity saturation region, the trans-conductance stays at a constant value $\gtrsim(\varepsilon_{ox}/T_{ox})WV_{sat}$ as the channel length is decreased, but the gate to channel capacitance C_{GC} decreases.

As the result, ω_c in the equivalent circuit increases linearly as the channel length decreases.

Then, as the design principle, the effort must be concentrated on the reduction of the channel length and the minimization of the drain to the gate feed back capacitance.

Ⅲ. Experimental fabrication

To assure the prescribed new concept, both types of transistors are experimentally fabricated.

The process flow chart is shown in Fig. 6.

The starting materials are polished and chemically etched n^- type 1Ω-cm (100) Si wafers or n^- on n^+ epitaxial wafers. 8000Å thick oxide is thermally grown for the diffusion mask and reduction of the stray capacitance.

Two step method is used for the p type base region formation. After the predeposition, the drive-in is carried out to the depth of 1μ in the oxidizing gas flow for the non-planar type and in N_2 gas flow mixed small fraction of O_2 gas for the plana rtype.

Prior to the phosphorous diffusion of the source region, the thin oxide grown during the base driver-in non-preferentially etched for the case of the planar type.

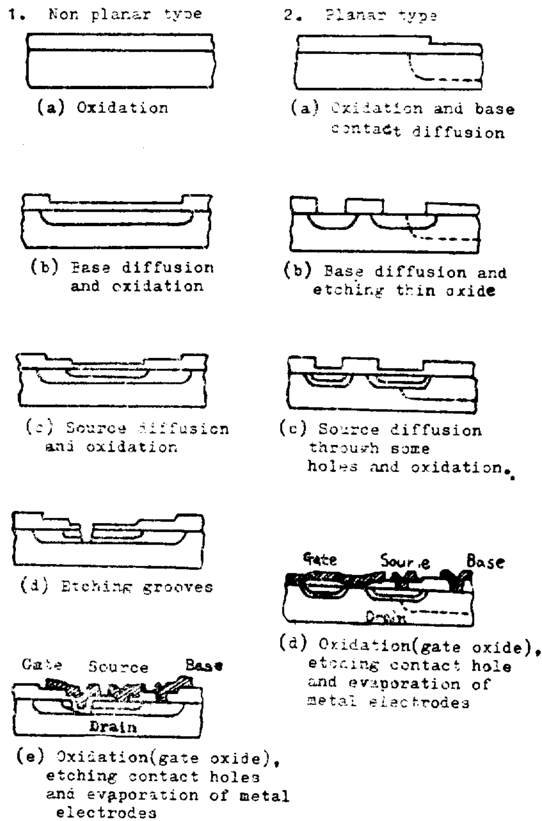


Fig. 6. Process flow chart of DSA-MOST (a) non-planar type, (b) planar type

The grooves of the non-planar type are etched to the depth of 1∼1.5μ using the oxide grown after the phosphrous diffusion as the mask. The preferen ial etchant is used for the reproducibility.

The gate oxide is thermally grown in the water vapor and treated in the phosphorous oxide vapor. The aluminum electrode for the non-planar type is evaporated about 1μ thick from evaporation source. The cross-section of the non-planar type is shown in Fig. 7, showing the channel length of 0.6μ along the etched grooves.

The bonding pad of the gate electrode is electrically shielded from the drain by the base layer.

The planar type shows also a similar geometry but no etched grooves and the fabrication is much easier. The channel length can be made shorter by adjusting the diffusion time.

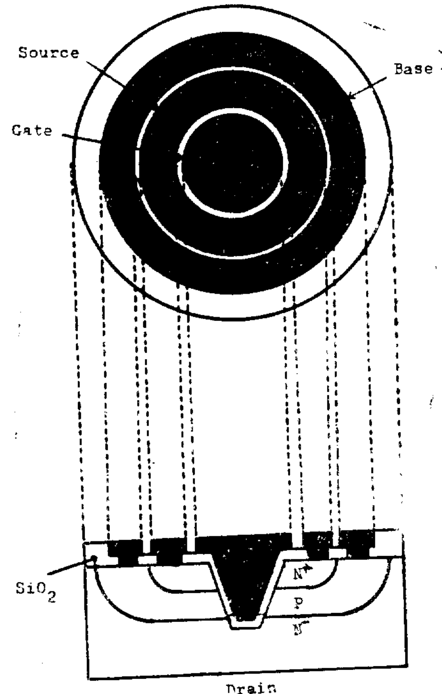


Fig. 7. Cross section of experim ntally fabricated DSA MOST -non-planar type-

The important fabricating conditions of DSA MOST are shown in table 1.

Table. 1.

Wafer	resistivity : 1Ω-cm, thickness : 0.4 mm, type: N-type, orientation : (100)

Field SiO_2	900°C steam oxidation : 100min. N_2 gas baking : 10 min.
Base diffusion	p type impurity : B_2O_3 1g diffusion time : 135min. impurity temperature : 700—900°C
Source diffusion	N type impurity : PCl_3, carrier gas : N_2 gas, N_2 gas flow rate : 1.5/min. PCl_3+N_2 gas flow rate 0.1l/min. impurity temperature; 28±1°C predeposition : 30min. diffusion time : 90min.
gate SiO_2	900°C steam oxidation : 30min. N_2 gas baking : 10min. thickness : 900Å
electrode fabricating	evaporating source : Al (99.9%) vacuum level : 1.6×10^{-5}mm Hg

IV. Electrical characteristics

The output characteristics of the fabricated DSA MOST's are shown in Fig.8.

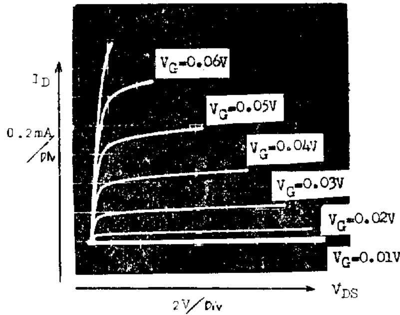


Fig.8. Output characteristics of the experimentally fabricated DSA MOST.-non-planar type-

The measured capacitances of the respective part of the non-planar type MOST is listed in table 2.

Table. 2.
measured capacitances of a non-planar type device.

C_{GC}	0.16
C_{GD}	0.064
C_{DB}	3.76
C_{GS}	1.00
C_{SB}	6.1

unit; pF

where

C_{GC} : gate-channel capacitance

C_{GD} : gate-drain capacitance

C_{GB} : drain-base capacitance

C_{GS} : gate-source capacitance

C_{SB} : source-base capacitance

It is noted that the drain to the gate feedback capacitance is as small as 0.064 pF.

Using these values, the cut-off frequencies defined in the chapter II are calculated as follows.

$f_c=15.92$ GHz

$f_r=19.9$GHz

$f_t=15.4$GHz (frequency at which equation (14) equals unity and stability factor less than unity)

The measured values are in good agreement with the theoretical values calculated from the geometrical structure.

These values are about one orders of magnitude higher than the cut-off frequency the high output conductance and breakdown voltage. No disastrous punch-through current is observed. The forward transfer conductance is typically 8m℧ for the non-planar of the biplor transistor which has the same dimensions.

It's interesting to note that the experimentally obtained devices with forward source-base bias condition show the bipolar operation and the gate voltage controles directly the charges in the operating base region. It is also noted that the compatibility in the fabrication of the high frequency MOST and the bipolar transistor will give the higher order of flexibility to the integrated circuit design.

V. Discussion and conclusion

The cut-off frequency of the device can be improved towards the theoretical limitation by optimizing the resistivity of the base region and the geometry. The voltage amplification factor is also made higher by the use of high resistivity epitaxial wafer.

The limitation of the channel length L is the same

with the channel length of few hundreds Å may be possible. The combination of the diffusion self-alignment technology with the precise pattern formation by the electron beam technology[1] will result in better designability.

The diffusion self-aligned MOST is proposed. This new construction realizes ultra high speed MOST's. The theoretical prediction and the result of the experimental fabrication promise the realization of tens of GHz MOST.

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