論 文
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A Study on the Energy Distribution of Interface Traps in MOS Devices Under Non-Steady-State

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Abstract

The phenomenon of non-steady-state current flow through the interface traps during the dielectric relaxation of MOS device is presented. Experimental method is also described for determining the energy distribution of interface traps, which is based on isothermal dielectric relaxation current technique. Actually, the energy distribution of interface traps was obtained by measuring the transient current through the traps at $Si\text{-}SiO_2$ interface only in lower-half of the bandgap. It is shown that the trap energy distribution has peak value 1.72×10^{13} cm^{-2} eV^{-1} near 0.73eV approximately.

I. INTRODUCTION

The planar technology and semiconductor devices made by this technology were first described in 1960. As the planar technology has, since, become the principal method of fabricating semiconductor devices and integrated circuits, the reliability and stability of semiconductor devices are intimately related to their surface conditions. It has been predicted theoretically by Tamm and Shockley that because of disruption of the periodicity of the lattice at a surface, a high density of states will be introduced into the forbidden gap near or at the semiconductor surface.(1)(2)

Several methods have been used to determine the density of surface states at the $Si\text{-}SiO_2$ interface of the MOS System [3]-[5],[7][8]. Most of these methods are made under steady-state or quasi-steady-state condition: Then the analyses of the data obtained by these methods are indirect and consequently are often tedious and subject to error. The limitations on the informationthat can be obtained from some of these methods have been discussed by Zaininger and Warfield(9) and Frankl(6).

Very recently, the effect of interface traps on the properties of MOS devices under non-steady-state Conditions has been discussed.(12)~(19) In this paper the isothermal dielectric relaxation current technique is used to study emission and surface generation throughout the interface traps at the $Si\text{-}SiO_2$ interface of MOS device. The emission current vs. time and the surface generation current vs. time characteristic are obtained in terms of the trap distribution throughout the entire bandgap theoretically and experimentally. Consequently. the energy distributions for interface traps are obtained from the current-time characteristic using the transformation equations, that is, a continuum of interface traps is obtained

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across the bandgap.

Ⅱ. THEORY

The MOS device is biased into the accumulation mode so that the interface traps in the upper-half of the bandgap will be filled to an energy, E_1 at which the Fermi level intersects the semiconductor surface(Fig.1-a). Next the device is in the inversion mode provided the gate is negatively biased. In this case, under quasiequilibrium conditions only those are filled that lie in levels below the energy, E_2 at which the Fermi level intersects the surface in the lower-half of the bandgap(Fig.1-d). Thus, when the sample is switched from the accumulation to the inversion mode, the interface traps located between the energy E_1 and E_2 lose their electrons. This relaxation process does not occur instantaneously, and during the period itoccurs, the device is in the non-steady-state. Under these conditions the initial relaxation mode is by the emission of electron from the interface traps, and finally by surface or bulk generation; Electrons escape from the interface traps in the upper-half of the bandgap by thermal excitation into the conduction band (Fig.1-b). When these traps have emptied, surface or bulk generation of electron-hole pairs becomes significant. In this event, electrons in the traps located in the lower-half of the bandgap escape by recombining with the generated holes in the valence band (Fig.1-c). The electrons that are emitted to the conduction band are immediately swept out of the depletion region by the high field therein into the neutral region, causing a current to flow into the external circuit. The system reaches quasi-equilibrium when the energy of the uppermost filled interface trap, E_{tn}^* coincides with the Fermi level in the bulk, Here we will be concerned with the emission current and surface generation current.

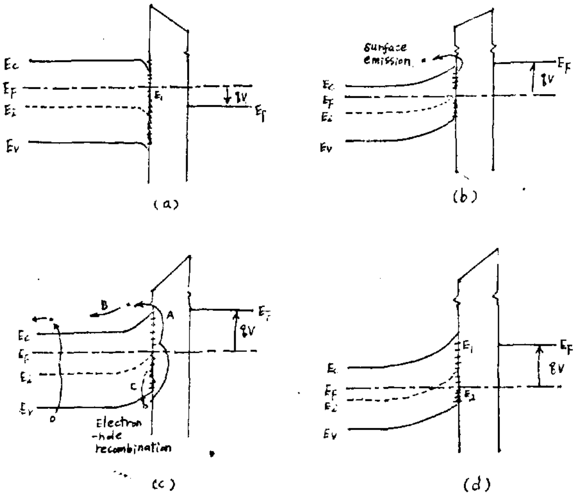

Fig. 1. Energy diagrms of an n-type MOS device
(a) the accumulation mode (b) the non-steady-state mode during surface emission of trapped electrons from interfacetraps in the upper-half of the bandgap. (c) the non-steady-state during surface and bulk generation of electron-hole pairs and the recombination of electrons trapped in the interfacetraps in the lower-half of the bandgap with holes in the valence band. (d) the quasi-equilibrium inversion mode.

II-1. NON-STEADY-STATE STATISTICS

In this section the non-steady-state statistics are derived for traps at the silicon-silicon dioxide interface when the device is switched from the accumulation mode to the inversion node. It has been shown that the rate equation that describes the trap occupancy at some time at an energy level is, according to the Shockley-Read Statistics, given by.10)11)

$$\frac{df}{dt}=(e_p+\overline{n})-(e_n+e_p+\overline{n}+\bar{p})f \qquad (1\text{—}1)$$

Now under reverse-biased conditions, the density of free electrons in the conduction band at the interface is small and may be neglected. However, the density of free holes at the interface cannot be neglected when the device is approaching the inversion mode. Thus, eq. (1—1) may be simplified to.

$$\frac{df}{dt}=e_p-(e_n+e_p+\bar{p})f \qquad (1\text{—}2)$$

The solution for the non-steady-state occupancy is found to be given approximately by

$$f(t)\simeq\left(f_0-\frac{e_p}{e_n+e_p+\bar{p}}\right)^{e^{-\lambda}}+\frac{e_p}{e_n+e_p+\bar{p}} \qquad (1\text{—}3)$$

where f_0 represents the initial occupancy of the traps at an energy and λ is given by

$$\lambda=\int_0^t(e_n+e_p+\bar{p})dt \qquad (1\text{—}4)$$

when the time is sufficiently short that the generation of free carriers is negligible, the energy level E_{tn}^* defined by $\lambda=1$ at a given time $t=t_1$

$$e_n(E_{tn}^*)\simeq 1 \qquad (1\text{—}5)$$

may be considered to represent the non-steady-state Fermi level for electrons in the upper-half of the bandgap. It will be shown in Fig.2 that in the upper-half of the bandgap it has a similar functional dependence on energy as that of a Fermi-Dirac distribution function. Thus it follows that for E_{tn}^* greater than about $2kT$ above midgap, the second term on the right-hand side of (1—3) may be neglected. Hence, in the upper-half of the bandgap $f\simeq f_0e^{-\lambda}$ and the statistics are governed only by the emission process. As the time increases, E_{tn}^* approaches the midgap energy E_i, which means that interface traps above E_{tn}^* have been emptied by the emission process. At sometime tc which E_{tn}^* reaches midgap, the function becomes sharply peaked about E_{tn}^* and collapses rapidly about E_i for any further increase in time. Hence, the emission process ceases and the generation process takes over. Thus, for $t>t_c$ the non-steady-state occupancy for the interface traps is given by

$$f(t)\simeq\frac{ep}{e_n+e_p+p} \qquad (1\text{—}6)$$

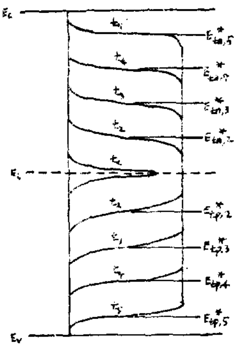

Fig. 2. The non-steady-state occupancy function $f\sim e^{-\lambda}$ in the upper-half of the bandgap.

II—2. DERMINATION OF TRAP DITRIBUTION

We will show that the product of the isothermal current and time plotted as a function of log t actually yields directly the interface trap distribution.

(1) EMSSION PROCESS

The emission current is related to the rate at which the traps are emptied, that is

$$I=\frac{qAC_o}{C_o+C_d}n_t=\frac{qAC_o}{C_o+C_d}\int_{E_v}^{E_c}N_{st}(E)e_n\exp(-e_nt)dE \qquad (2\text{—}1)$$

$Eq(2$—$1)$ may be solved approximately for any trap distribution⁽¹⁴⁾~⁽¹⁶⁾

$$I=\frac{qAC_o}{C_o+C_d}N_{st}(E_{tn}^*)\frac{kT}{t}(1-e^{-\nu t}) \qquad (2\text{—}2)$$

The attempt-to-escape frequency ν is usually of the order 10^{11} to 10^{12} $\sec^{-1}$ hence, $e^{-\nu t}$ is much smaller than unity for realistic values of t. In practical MOS devices in the deep-depletion mode $C_d\ll C_o$, so that (2—2) reduces to

$$N_{st}(E_{tn}^*)=\frac{It}{qAkT} \qquad (2\text{—}3)$$

which shows that the product of current and time is linearly proportional to the occupied trap density at E_{tn}^*. Furthermore, E_{tn}^* is related to the time by

$$E_c-E_{tn}^*=kTl_n\nu t \qquad (2\text{—}4)$$

$$\text{or } E_c-E_{tn}^*=2,3026\ kT(\log t+\log\nu) \qquad (2\text{—}5)$$

Hence, using (2—5) the log t axis can be transformed into energy measured with respect to the bottom of the conduction band. In other words, using the transformations provided by (2—3) and (2—5), the I t vs. log t characteristic may directly converted into the $N_{st}(E'_n{}^*)$ vs. E_c—E_{tn}^* characteristic, that is, into an actual plot of the interface trap distribution.

(2) GENERATION PROCESS

The total rate of surface generation of electron-hole pairs through the interface traps is given by

$$\dot{n}_t=\int_{E_v}^{E_c}\frac{e_ne_p}{e_n+e_p+p}N_{st}(E)dE \qquad (2\text{—}6)$$

Thus the surface generation current is given by [17], [18]

$$I=\frac{qAe_ne_p}{\bar{p}}\int_{E_{tp}^*}^{E_{tn}^*}Nst(E)dE \qquad (2\text{—}7)$$

Furthermore $E_{tp}^*(E)$ is related to the time by [17], [18]

$$E_{tp}^*(E)=E_g-kTl_n\left(\frac{v_{th}\sigma_nN_c}{kT}\ \frac{\int_{E_{tp}^*}^{E_{tn}^*}N_{ts}(E)dE}{N_{st}(E_{tp}^*)}\right)$$
$$-kTl_nt \qquad (2\text{—}8)$$

If we examine (2—8), it will be assumed

that $E_{tp}{}^*$ is essentially a linear function of ln t provided that the factor R in the argument of the logarith varies only slowly with time.

$$R=\int_{E_{tp}{}^*}^{E_{tn}{}^*} N_{st}(E)dE/N_{st}(E_{tp}{}^*) \qquad (2-9)$$

Hence, eq. (2—8) is found to be a good approximation to [18]

$$E_g-E_{tp}{}^*=kTl_n\left[\frac{1.8\times10^3\nu t}{T}\right] \qquad (2-10)$$

Also, eq(2—7) can be rewritten as

$$N_{st}(E_{tp}{}^*)=\frac{It}{qAkT} \qquad (2-11)$$

Therefore using the approximately linear relation between $E_{tp}{}^*$ and time given by(2—10), the time axis can be transformed into an axis representing energy above the top of the valence band. It will be apparent from(2—10) and(2—11) than the I t vs. ln t plot is a direct image of the interface trap distribution in the lower-half of the bandgap.

Ⅲ. EXPERIMENT

The sample used in the experiment is an MOS structure, in which the oxide layer thickness is 1150Å. The substrate is n-type silicon of 8~12 Ωcm resistivity The area of the metal gate is 1.23×10^{-2}cm². The elements of a circuit for performing a measurement are shown in Fig.3. This circuit is essentially an analog differentiator incorporating the MOS device as a capacitive element. This circuit may beconveniently realized using an electrometer such as the TAKEDA RIKEN MODEL TR-8651. The sample is measured within a chamber box such as the DAKEDA RIKEN MODEL TR-42 to isolate electrical leads and feeds are also shielded against electrical disturbances. The temderature of the sample was measured using a temperature chamber such as CO_2—25 TYPE.D.C. voltage source provides the bias-voltage in the form of the step voltage The transient current is observed to flow through oscilloscope such as TELEQUIPMENT STORAGE TYPE DM-64. At the same time this current is recorded by X-Y recorder (YEW TYPE-3077) automatically and continuously.

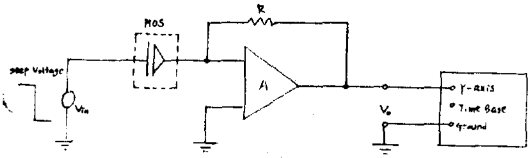

Fig. 3. Equivalent Circuit for I vs. t measurement

Ⅳ. RESULTS AND DISCUSSION

Fig4-Fig 7 illustrate a family of transient current characteristics. The initial and final voltage biases used through the experiments were 6V (accumulation state) and −16V(inversion state). Since the measurement circuit shown in Fig 3. is a simple differentiatior circuit, the output of the electrometer is expressed by $V_{out}=-RY_{in}\frac{dc}{dt}$. The resistance R, which is the standard resistance of the electrometer, can be chosen from 10^5 to 10^{11} ohms according to the measurement range. The current can be obtaned by normalizing the output votage with the standard resistance. The current that circulates the external circuit after the voltage step (or pulse) is applied comprises four main components; surface emission (I_e), surface generation (I_s), bulk generation(I_{gb}) and depletion current(I_d). The latter is a displacement current arising from the change of the depletion charge as the depletion region changes in width. Thus, the total current I is given by

$$I=I_e+I_{gs}+I_{gb}+I_d$$

It can be shown [15] that the total current may be rewritten in the form

$$I=\frac{C_o}{C_o+C_d}(I_e+I_{gs}+I_{gb})$$

Cd is generally much smaller than the oxide capacitance Co, so

$$I\simeq I_e+I_{gs}+I_{gb}$$

By altering the initial conditions, the transient current vs. time characteristics exhibits different shapes, which enable one to distinguish between surface emission, surface generation and bulk generation processes. Actually, when the device is initially biased into the accumulation, the early portion of the transient response is due to emission of electrons from interface traps with energy above the middle of the badgap. At a later time, the emission process, gradually gives way to surface generation, which completely dominates the emission process at $t=0.25\sim0.3$ sec.

At room temperature the trapped electrons escape in less than 10^{-3}sec after the device has been biased into the deep-depletion mode, which time is less than the response time of the electrometer. Thus, at $t=2.5\sim3.0$sec, that is, where the surface-generation process dominates, the I-t curve is directly proportional to the trap distribution in the lower-half of the bandgap. From the experimental curve the relation of theinterface trap density and energy can be directly obtained using the transformation (2—3), (2—5) and (2—10), (2—11).

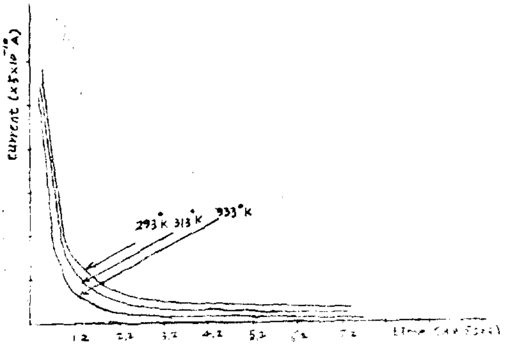

Fig. 4 I vs t curve (1)

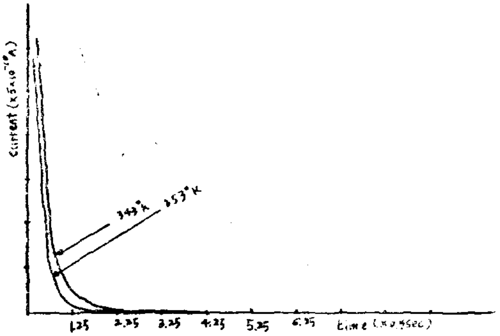

Fig. 5 I vs. t curve (2)

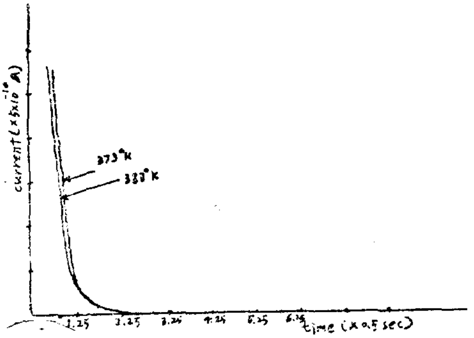

Fig. 6 I vs. t curve (3)

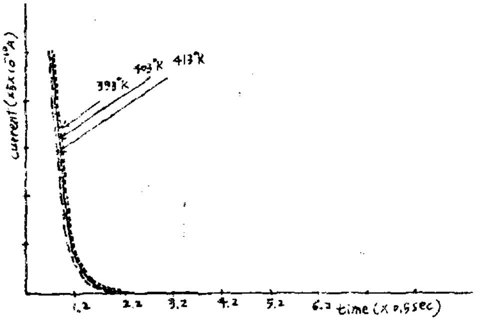

Fig. 7 I vs. t curve (4)

To analyze the experimental data in the manner described above we need know the value of the attempt-to-escape frequency. This parameter may be obtained by plotting the It-log t characteristic at two different temperatures T_1 and T_2. Then by measuring the time t_1 and t_2 on the T_1 and T_2 at which the peak point of the characteristic occurs, corresponding to an energy the attempt-to-escape frequency may be determind. We show the results of Fig.4—7 transformed into the trap distribution using transformation equations in Fig.8. It is seen that the trap distribution has peak value with maximum of 1.72×10^{13}cm^{-2}eV^{-1} situated 0.73eV respectively, below the bottom of the conduction band.

In fact, it is theoretically expected that the trap distribution has two peaks:the first(higher-energy) peak lies in the upper-half of the bandgap while the second peak (lower-energy) lies in the lower-half of the bandgap. Thus, they are thought to emission and generation peaks respectively. But because of the limit of temperature variation, the complete data were not until obtaind. Furthermore, the experiment is being carried out.

Table. Parts of $N_{st}(E)$ vs E_t-E_v data.

	293°K	303°K	313°K	333°K	353°K	363°K	373°K	403°K
E_t-E_v	0.725	0.750	0.774	0.8226	0.871	0.895	0.920	0.992
$N_{st}(E)$	17.2×10^{12}	16.3×10^{12}	15.2×10^{12}	14.3×10^{12}	13.5×10^{12}	11.4×10^{12}	10.7×10^{12}	8.33×10^{12}

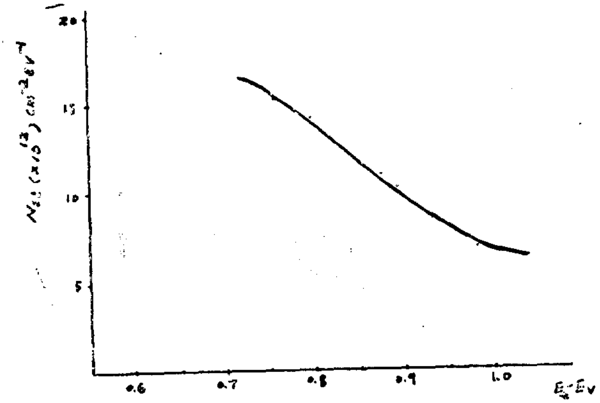

Fig. 8 $N_{st}(E)$ vs E_t-E_v

V. CONCLUSION

The energy distribution of interface traps in MOS device was obtained in the lower-half of the bandgap. The trap distribution has peak value with maximum of 1.72×10^{13} cm^{-2} eV^{-1} situated 0.73eV respectively, below the conductionband. Also. it is thought that IDRC technique provides a simple method of measuring the trap energy distribution across the entirebandgap of MOS System.

REFERENCES

1) A. Many, Y. Goldstein, N.B. Grover, Semiconductor Surfaces, American Elsevier(1971)

2) S.M. Sze, Physics of Semiconductor Devices, Wiley(1969)

3) L.M. Terman, "An Investigation of Surface States at a Silicon/Silicon oxideInterface employing]MOS Devices", Solid State Electron, 5, 285 (1962)

4) C.N. Berglund, "Surface Ssates at Steam-Grown Silicon Dioxide Interface," IEEE. Trans. ED-13, 701 (1966)

5) P.V. Gray, D.M. Density of SiO_2-Si Interface States", Appl. Phys. Letts. 8, 31 (1966)

6) D.R. Frankl, "Comment on Density of SiO_2-Si Interface States by Gray and Brown," J. appl. Phys. 38, 1996(1967)

7) E.H. Nicollian, A. Goetzberger, "The Si-SiO_2 Interface Electrical Properties as Determined by the MIS Conductance Technique", BSTJ 46, 1055(1967)

8) M. Kuhn, "A Quasi-Static Technique for MOS C-V and Surface States Measurements", Solid State Electron, 13, 873(1970)

9) K.H. Zaininger, G. Warfield, "Limitations of the MOS Capacitance Method for the Determination of Semiconductor Surface Properties" IEEE. Trans. ED-12, 179 (1965)

10) W. Shockley,pW.T. Read, "Statistics of the Recombinations of Holes and Electrons,"Phys' Rev. 87, 835(1952)

11) J.G. Simmons, G.W. Tayor, "Nonequilibrium Steady-State Statistics and Associated Effects for Insulators and Semiconductors Containing an Arbitrary Distribution of Traps," Phys. Rev. 134, 502 (1971).

12) J.G. Simmons, H. A. Mar, "Thermal Bulk Emission and Generation Statistics and Associated phenomena in Metal-Insulator-Semiconductor Devices Under Non-Steady-State Conditions", Phys. Rev. B8, 3865(1973)

13) L.S. Wei, J.G. Simmons, "Transient Emission and Generation Currents in Metal-Insulator-Semicondutor Capacitors",Solid State Electron 18, 853 (1975)

14) J.G. Simmons, M.C. Tam, "Theory of Isothermal Currents and the Direct Determination of Trap Parameters in Semiconductors and Insulators Containing Arbitrary Trap Distributions." phys. Rev. B7, 3706(1973)

15) J.G. Simmons, L.S. Wei, "Theory of Transient Emission Current in MOS Devices and the Direct Determination Interface Trap Para-

meters", Solid State Electron, 17, 117 (1974)

16) J.G. Simmons, G.W. Taylor, "Theory of Non-Steady-State Interfacial thermal Currents in MOS Devices and the Direct Determination of Interfacial Trap Parameters", Solid State Electron, 17, 125(1974)

17) H.A. Mar, J.G. Simmons, "Surface-generation Statistics and associated thermal Currents in Metal-oxide-Semiconductor Structures", Phys. Rev. B11, 775(1975)

18) J.G. Simmons, H.A. Mar "Tansient isathermal Generation at theSilicon-silicon dioxide interface and the Direct Determination of Interface Trap Distribution," Solid State Electron, 19, 369(1976)

19) H.A. Mar, J.G. Simmons, "A Review of the Techniques used to Determine Trap Parameters in the MNOS Structure", IEEE. Trons. ED-24, 540 (1977)