

Wook Rang Shim  
(沈旭郎)

# Application of Microprocessors to Communication System

## Abstract

The use of a Microprocessor and PROM memories in an Electronic Loop Switching System has been described. The use provides telephone service for up to 128 subscriber lines using 32 trunks with increased reliability, maintenance capabilities, and flexibility. Data Communication between the central office terminal and the remote terminal is by FSK at 1-KHz rates over an idle trunk. Software functions and traffic handling capabilities are also described.

## I. Introduction

The line concentrator of telephone systems consists of two terminals, the central office and remote terminals, and utilizes outside plant cable facilities more efficiently.

Early line concentrators with an entire electro-mechanical system are physically large, mechanically complex and difficult to maintain due to the absence of a self-diagnostic capability.

The next generation of concentrators utilized a digital system to control an electromechanical switching network. This increased reliability and allowed certain maintenance features. The size was dramatically reduced, but the control by a minicomputer is not practical.

Microprocessors consisting of a few Large Scale Integrated (LSI) circuits and performing the basic functions of a central processing unit, input, output and arithmetic operations, are a new and efficient tool to control the switching network of the concentrator. The microprocessor, with digital control circuits, greatly reduces the number of components and in turn increases reliability. They are programmed to detect, diagnose or analyze system faults and to display any trouble utilizing a trouble code. Therefore, it is highly efficient in achieving substantial maintenance features although terminals are separated by a distance of several miles.

Nevertheless, there is a disadvantage associated with the use of microprocessors for a system design. They require the designer to learn how to write machine language programs in addition to performing hardware design. The advantages offered by microprocessors and their use with switching systems will be described in the following sections.

## II. Electronic Subscriber Switching System

Figure 1 shows an electronic subscriber switching system currently under development by

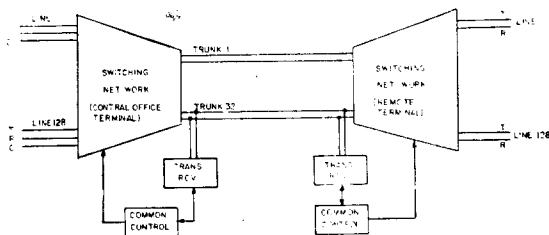


FIG. 1 Block diagram of a Subscriber Switching System

Lynch Communication Systems, Inc. Current design utilizes two Intel 8008-1 microprocessors. The system provides the use of 128 subscriber lines at a remote terminal using a maximum of 32 trunks without modifications to a central office. Physical cable pairs or existing current carrier channels can be used as trunks between terminals. Automatic Number Identification (ANI) equipment and billing systems may still be used without any other additional equipment. T.R.

\*Lynch Communication Systems, Inc in Reno, Nevada, U.S.A. Senior Design Engineer

and C-leads of subscriber lines at a central office terminal are directly connected to Main Distribution Frame (MDF).

The system can handle up to eight intra-call remote connections allowing as many as eight called parties to be connected to eight calling parties without using the trunks between two terminals. This feature, which improves traffic handling capability, provides for verification of busy lines. Verification of an intra-call can be performed at a central office because the trunks of calling parties are connected to the frame of the central office. The switching network of the system is a two stage latching relay switching matrix providing 64 links as shown on Figure 2.

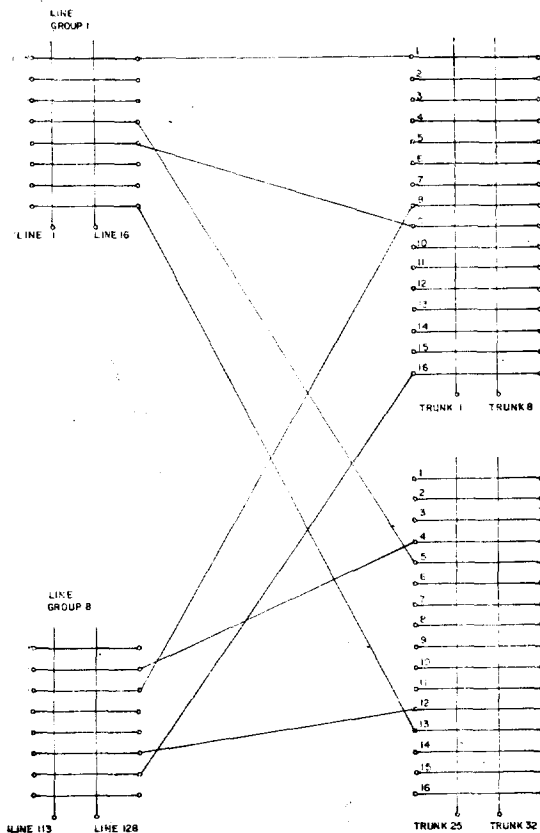


FIG. 2 64 LINKS OF SWITCHING SYSTEM

### III. Data Communication

It is very important for any split system to get

a great reliability in data communication. The transmitter and receiver is a half-duplex system using Frequency Shift Keying (FSK) signaling with a 1-KHz bit rates. The parallel digital format is converted to serial sinusoidal frequencies: 1200Hz for mark and 2200Hz for space.

The message format is composed of a 4-millisecond start pulse followed by 24 1-millisecond bit time slots: 16 bits for data information and an 8-bit error correcting word. The message is loaded in 8-bit bytes to a transmitter and receiver which contains an LSI chip known as UART, "Universal Asynchronous Receiver Transmitter." This circuit automatically inserts necessary start, stop and parity bits. It also performs framing and parity checks, thus relieving the microprocessor of this task when a message from a sending terminal has been received.

The error correcting word is used to detect errors consisting of more than one bit of information. The complete received message is retransmitted back to the sending terminal where it is compared bit by bit with the message originally transmitted. If two messages do not match, the sending terminal will retransmit the message. If the failure to successfully transmit a message continues with three attempts, a trouble code will be displayed and reselection of another trunk for data communication is achieved. This can be done because the terminals are in constant communication over an idle trunk.

With redundancy of checking by the microprocessor and retransmission, combined with alternate selection of trunks, greater increased reliability in data communication, is obtained.

### IV. Intel 8008-1

Integrated Circuit (IC) technology developed in early 1960's has made dramatic advances. For digital and analog systems, this technology has proven to be particularly appropriate for manufacturing circuit elements such as gates, flip-flops, multiplexers, latches and operational amplifiers. A digital computer can be implemented with a few IC chips. Therefore, minicomputers

have produced a revolution in design and test of systems.

Finally, this technology has expanded to make microprocessors exhibit even greater revolution in the use of digital processing.

Three kinds of microprocessors contain either 4-bit, 8-bit, or 16-bit parallel central processing units. The choice of the Intel 8008-1 is made on the basis of speed, programming flexibility and size. The microprocessor can execute non-memory referencing instructions in 12.5 microseconds. The programming flexibility of microprocessors are more suitable for complex control functions required by a switching system. The 8-bit microprocessor is most appropriate to the application because it will rapidly control a 128 line subscriber loop switching system with speed and has facilities for forming the 8-bit data messages that must be transmitted back and forth between two terminals. Figure 3 shows the block diagram of the 8008-1. The 8008-1 is a single chip, 8-bit Central Processing Unit (CPU) consisting of six registers, one 8-bit accumulator, two temporary registers (one to develop four discrete flags and the other for binary arithmetic

The instruction set for machine language programming of the 8008-1, consists of 48 instructions including manipulation, binary arithmetic operations and call to subroutines. These instructions are well explained in the 8008 8-bit Parallel Central Processor Unit, Users Manual.

The normal program flow of the microprocessor is interrupted by the interrupt control. The state of the processor at any time in the instruction cycle is indicated by S0, S1, S2 and SYNC as shown on Figure 4. A machine cycle, consisting of five timing states T<sub>1</sub>, T<sub>2</sub>, T<sub>3</sub>, T<sub>4</sub> and T<sub>5</sub> controls the CPU state transitions. These are illustrated on Figure 5. The processor is driven by a two phase nonoverlapping clock. The two clock periods are required for each state of the

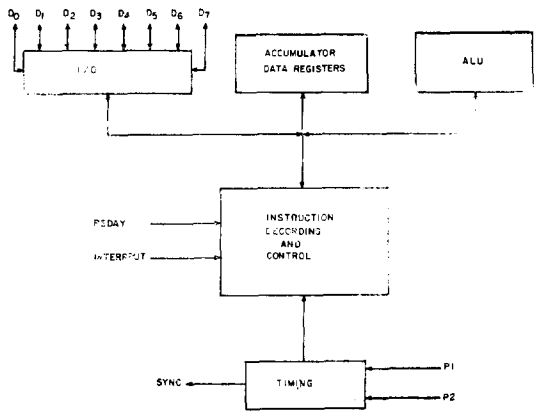


FIG 3 Block diagram of the Intel 8008-1.

operations), two dynamic memories (a push down stack address and a scratch pad), and I/O buffer.

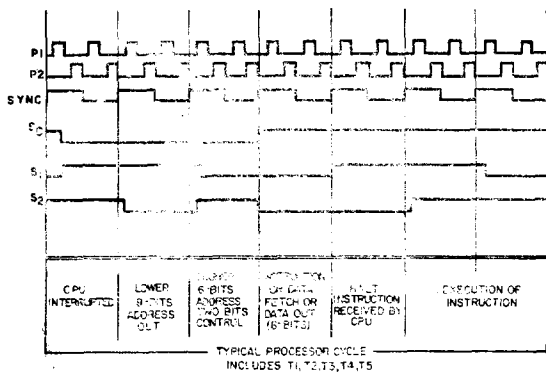


FIG. 4 INSTRUCTION CYCLE OF 8008

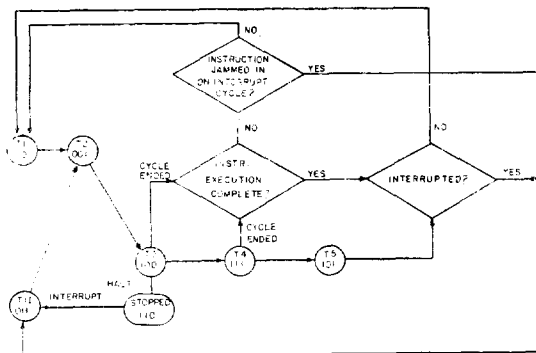


FIG 5 CPU State Transition Diagram

processor. A SYNC signal is generated by the processor is the signal divided two of P2 shown on Figure 4.

### V. Common Control Unit

The hardware of each of the common control units at each terminal is identical, although the software is slightly different. The common control is consist of six modules; they are the CPU, input port, output port, memory, maintenance routine, and keyboard-display modules as shown on Figure 6.

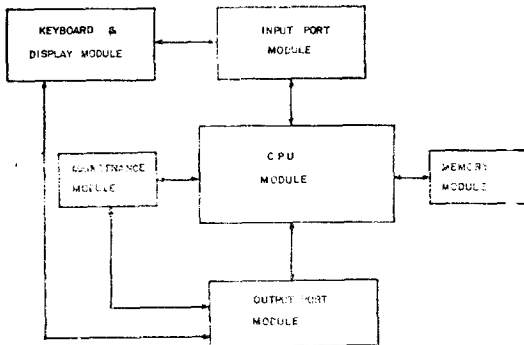


FIG. 6 Block diagram of Common control Modules

#### A. CPU Module

The CPU contains the 8008-1 logic circuits required to decode the status of the processor, address registers and an 8-bit data bus. To prevent the possibility of component malfunction causing a closed loop in the computer program, a hardware timer is incorporated in the CPU module. When a time out occurs, the interrupt command generated by the CPU forces the program counter to the program address routine which clears and restarts the system. Also, the trouble codes will appear on the display module.

#### B. Memory Module

The memory module contains two 4K-Read Only Memories (ROM), eight 2K-Programmable Read Only Memories (PROM) and eight 1K-Random Access Memories(RAM) as shown on Figure 7. All program is stored in ROM and PROM. RAM is used as a temporary scratch pad station to excute programs and store trouble

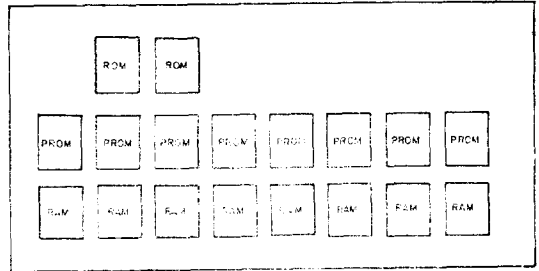


FIG. 7 Memory Module

codes. It is an advantage to use PROM memories because a program can be erased by ultraviolet light and reloaded by a designer. The processor with PROM memories increases the flexibility of a system.

#### C. Output Port Module

The output port module, which consists 16 four-bit latch chips, sequentially controls the switching unit and the data communication to programs. C-MOS chips are used for noise immunity. Data selector chips are incorporated to Select individual output ports under programming control.

#### D. Input Port Module

All information to the CPU from the data communication network, the line scanning output, the detection outputs of loop current and intracalling, malfunctions, and diagnostic results, are collected by this module. Data selectors are incorporated to select individual input ports under programming control.

#### E. Maintenance Module

The maintenance module monitors the output from the CPU, and verifies that the proper commands are transmitted to the remainder of the system. This module also controls routine checking regularly.

#### F. Display Module

Fig re 8 shows the display module. The display module located at the front of the system, consists of a four digit hexadecimal Light Emitted Diode(LED) display. This unit is used to display the traffic data, the trouble codes, and monitoring information whichever is requested to display by a keyboard punching. A trouble dictionary wil

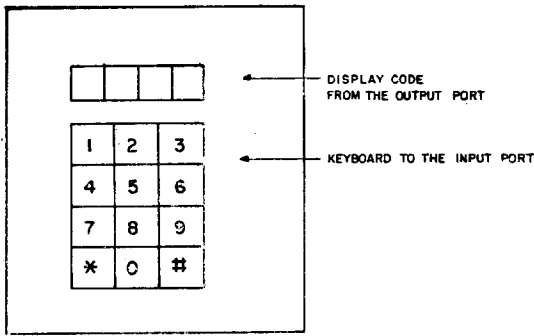


FIG. 8 DISPLAY MODULE .

be prepared for maintenance personnel.

### VI. Software

The system has enough flexibility to interface with all types of central offices throughout the world. The programming capability of a micro-processor and PROM memories provides this flexibility. The software of the system has six major segments: system initialization, data communication between two terminals, call processing, diagnostics, fault recovery, and system monitoring.

#### A. The system initialization

When the system is being powered up for the first time, all hardware and the tables of the system are cleared. Then, the data communication will be established. The initialization determines the configuration of the system by interrogation of the switching network for unequipped circuit modules and will update system tables to reflect the hardware configuration. The initialization performed by a restoral at one terminal, also makes the terminal refresh the software status tables of the system at the other terminal. In this manner, one terminal may lose power and automatically recover without causing the loss of any call in process.

#### B. Data Communication

This software is responsible for the forming and processing of messages between two terminals. When a received message for comparison is not matched with a transmitted data, this software sends signals to indicate trouble code handled by diagnostic software. Also, the signals

control call processing software to lock out the trunk until it is repaired.

#### C. Call Processing

The call processing software scans the lines or connection or disconnection requests. It also scans idle trunks for intra-call detection, and controls the path selection through the network switching. The various status tables of the system are refreshed and updated by this software. Also, it scans called party trunk for intra-call detection and disconnection. The connection and disconnection of intra-calls at a remote terminal is function of this software .

#### D. Diagnostics

When any trouble occurs, diagnostics isolates the fault, formats a trouble code, and places it in a queue for subsequent display. Also, it controls major alarm and minor alarm for maintenance personnel.

#### E. Fault Recovery

Fault recovery permits reconfiguration and recovery from a detected fault. It restores normal operational functions and reroutes fault conditions. Also, this software indicates to the subroutine program for refreshing tables.

#### F. System Monitor

The System monitor software formats messages from the other modules for display. It also formats the inputs from the key board and places them in queues for use by the appropriate module. This software monitors the trunk usage including total trunk usage, the number of blocking calls, and percentage intra-call for traffic study.

Each major software unit is made up of a number of subroutines which are shared among various softmodules. The capability of detecting, analyzing and rerouting around a fault, drastically reduces the possibility that a single fault will affect subscriber service.

### VII. Traffic Handling Capacity

The traffic handling capability of the system is a function of a number of trunks to the central office and subscriber line access of these

trunks. The capability depends on the percentage of intra-calling traffic as shown on Figure 9. The

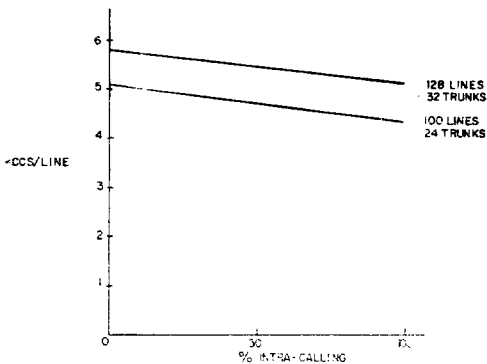


FIG 9 TRAFFIC HANDLING CAPACITY WITHOUT INTRA-CALLING SWITCHING AT REMOTE TERMINAL.

minimum traffic handling capacity is 4.5 CCS/LINE at .01 blocking rate with a full access, full availability switching system of 128 lines to 32 trunks as a function of the percent intra-calling. However, the capacity increases with an increased percentage of intra-calling by the addition of the intra-call switching at the remote terminal as shown on Figure 10.

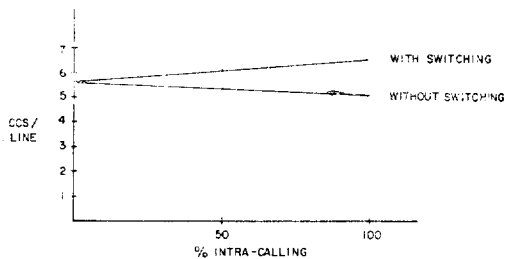


FIG 10 COMPARISON OF TRAFFIC HANDLING CAPACITY WITH AND WITHOUT REMOTE SWITCHING.

The traffic handling capacity on Figures 9 and 10 is calculated by the method of Poisson distribution. The Poisson distribution method of determining blocking versus applied load assumes that the applied load probability statistics have a Poisson distribution. If we take the case of 100 % intra-calling, we still assume that the applied load has a Poisson distribution, but the absolute number of trunks available to the handling of the load must now be considered to be one half the physical number since one trunk is never sufficient to complete a connection or handle any load. Two trunks are always needed in any

pairing to complete a call. The above idea has been advanced and put in practice by Bell Telephone Laboratories.

## VIII. Future

The system can handle as many as 128 subscriber lines with up to 32 trunks. If the subscriber lines at a remote excution were split (in other words, two remote terminals are used with one central office terminal), the use of the software would greatly increase such that the speed of the 8008-1 is not sufficient. In such a case the Intel 8080 and some additional digital circuit could be used to achieve this application. The 8080 can excute nonmemory reference instructions in a time as short as one microsecond.

## IX. Reference

1. Donald H. Hamsher, Communication System Engineering Handbook, New York : McGraw Hill, 1967.
2. N. Taub and D.L. Shilling, Principles of Communication Systems, New York: McGraw Hill, 1971.
3. F. Faggin, M. Shima, M.E.Hoff, H. Feeney and S. Mazor, "The MCS-4 An LSI Micro Computer System", IEEE, 1972, Region Six Conference, pp.1-6.
4. D.Frohman-Bentchkowsky, "A Fully Decoded 2048-Bit Electrically-Programable MOS-ROM", ISSCC Digest of Technical Papers, Feb. 1971. pp. 80-82.
5. William Roberts, "Microprogramming Concepts and Advantages as Applied to Small Digital Computers", Computer Design, November 1969, pp.147-150.
6. L.L.Vadasz, A.S. Grove, T.A.Rowe, and G.E. Moore, "Silicon Gate Technology", IEEE Spectrum, October 1969, pp.27-35.
7. R.N.Noyce, "A Look at Future Costs of Large Integrated Arrays", AFIPS, Vol. 29, 1966, FJCC, Spartan Books, pp. 111-114.
8. F.Coury, "A Practical Guide to Minicomputer Application", IEEE Press, New York, 1972, pp.71-95