3상 3레벨 태양광 PCS에서 누설전류 저감 기법

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Leakage Current Reduction by a New Combination of PWM Method and Modified connection for 3-level Inverter Photovoltaic PCS

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ABSTRACT

This paper presents the two combination methods for leakage current reduction in photovoltaic system PCS. The leakage current in the photovoltaic system generated from the parasitic capacitance existing between the photovoltaic system and ground relevance to common mode voltage caused by PWM switching. Firstly, Leakage current reduced by a PWM method using two carriers with 180-degree phase different. Secondly, the leakage current is more reduced by connecting LCL filter to the mid-point of DC link. This combining method is revealed in PSIM simulation with 1 uF parasitic capacitance.

I. INTRODUCTION

Electricity demand is increasing every single day in the world. In the past, electricity mostly generated from non-renewable energy like coal power plants which make a concern of the environment. But nowadays the world is interested to generate electricity from a renewable source such as hydropower, wind energy, and solar PV system. Among them, solar energy is being used widely in industry and home because it is easy to repair and can be used in a longtime. In the photovoltaic system PCS, the leakage current is caused by the common-mode voltage due to PWM switching and the parasitic capacitance of PV system. Leakage current is existing between the photovoltaic array and ground [1]. This leakage current is required to be reduced to solve the safety problems of the operator and the malfunctions of the protective relay and peripheral device [2].

Photovoltaic system topology that uses transformer is the one of typical method for reducing leakage current but the system increase the cost spending along with the size [3]. There are two methods in this paper presented to avoid using transformer. The first method is using a new PWM method which changes the phase of two carriers from conventional PWM. The second method is a new path which adding a connection from the LCL filter to the mid-point of DC link. In this paper, a leakage current reduction method with proposed SVPWM and modified connection be revealed in PSIM simulation. Moreover, the combination of proposed SVPWM and the bypass path method is the way to further reduce the leakage current.

II. EVALUATION of LEAKAGE CURRENT BASED ON EQUIVALENT CIRCUIT

Figure 1 shows the equivalent circuit of 3-phase 3-level NPC type inverter system with PV array and connected to the grid. The galvanic non-isolation of PV grounded array and the grid provide the possibility of leakage current circulation capacitance.

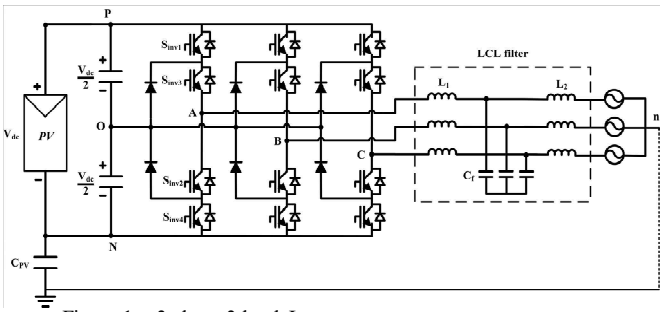


Figure 1 : 3-phase 3-level Inverter system

Figure 2 shows a leakage current equivalent circuit 3-phase 3-level inverter system with a parasitic capacitance C_{pv} of 1uF. This figure can be calculate common mode voltage by (1). The current of the parasitic capacitance can be calculate by (2).

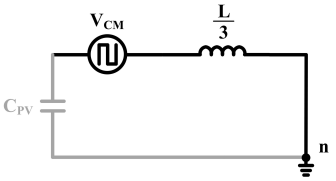


Figure 2: leakage current equivalent circuit.

$$V_{CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \quad (1)$$

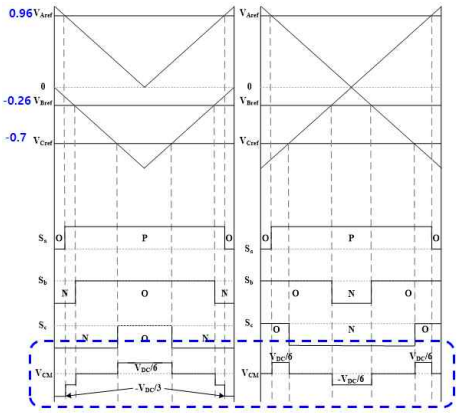
$$i_{Cpv} = C_{PV}\frac{d\,V_{PV}}{dt} \quad (2)$$

III. METHOD OF REDUCING LEAKAGE CURRENT

A. Proposed PWM method to reduce leakage current

The main feature of the proposed SVPWM is simple to implement, less switching losses and further reduced leakage current as compare to conventional SVPWM.

Figure 3 shows the comparison between conventional SVPWM and proposed SVPWM. The proposed SVPWM has 180-degree of phase difference between two carriers. In conventional SVPWM, (POO) and (ONN) generate $\pm V_{DC}/6$ and $\pm V_{DC}/3$ of common mode voltage, respectively. But proposed SVPWM has only (POO) which generates $+V_{DC}/6$ of common mode voltage.



(a) (b)

Figure 3: Comparison of SVPWM (a) Conventional SVPWM (b) Proposed SVPWM

B. Modified connection to reduce leakage current

Figure 4 shows a modified path that connecting the node of capacitor of LCL filter to the mid-point of DC link. The modified connection reduce the leakage current flow through capacitance C_{pv} in the system.

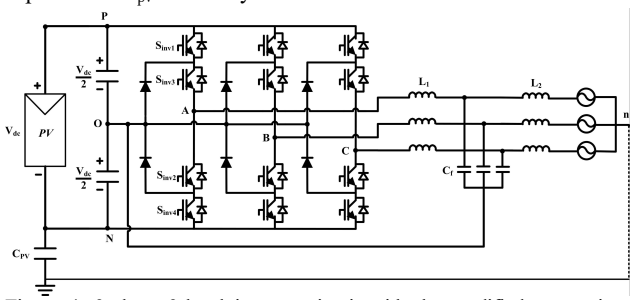


Figure 4: 3-phase 3-level inverter circuit with the modified connection.

IV. SIMULATION

This combining method is simulated in PSIM program with the parameter in table 2.

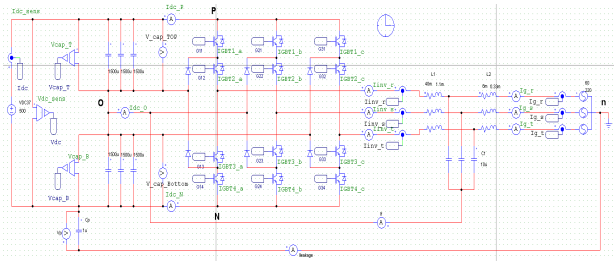
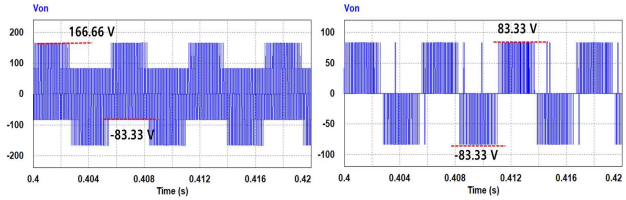


Figure 5: simulation schematic of 3-phase 3-level NPC inverter

Table 1: System parameter

Parameter	Symbol	Value
DC Source	V	**500 V**
Power	**P**	**5 kW**
Filter Inductance	L_1	**1.11 mH**
Filter Inductance	L_2	**0.33 mH**
Filter Capacitor	C_f	**10 uF**
Parasitic Capacitor	C_P	**1 uF**
Switching Frequency	f	**10kHz**

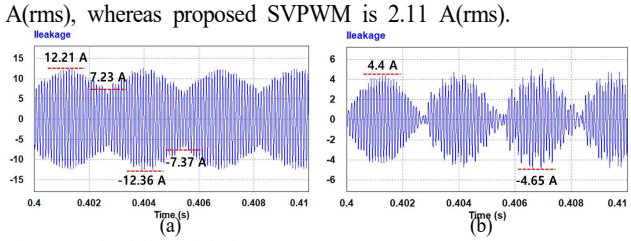
Figure 6 shows common mode voltage when parasitic capacitance is not considered. This simulation compares conventional SVPWM and proposed SVPWM, and the proposed SVPWM is $\pm 83.33\,V(\pm V_{DC}/6)$ and $0\,V$, respectively that is lower than conventional SVPWM.



(a) (b)

Figure 6: Simulation of common mode voltage (a) Conventional SVPWM, (b) Proposed SVPWM

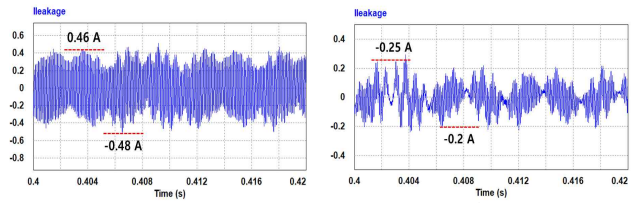
Firgure 7 shows leakage current waveform with parasitic capacitance considered. For conventional SVPWM is 7.04 A(rms), whereas proposed SVPWM is 2.11 A(rms).



(a) (b)

Figure 7: Simulation of leakage current (a) Conventional SVPWM, (b) Proposed SVPWM

Firgure 8 shows leakage current waveform on topology method. For conventional topology is 255mA(rms) and the proposed topology the value is 88mA(rms).



(a) (b)

Figure 8: Simulation of leakage current (a) Conventional topology, (b) Proposed topology

V. CONCLUSION

In the photovoltaic system, leakage current is produced by parasitic capacitance of PV array and common mode voltage of inverter. Two combined method which consists of new PWM and modified connection much reduced leakage current in the system. The proposed SVPWM reduced current from 7.04 A(rms) to 2.11A(rms). Meanwhile, leakage current was more reduced by using modified connection from the value 255mA(rms) to 88mA(rms).

REFERENCES

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