커패시터 전압 자기 밸런싱 기능이 있는 새로운 6-레벨 인버터 토폴로지

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A Novel Six-Level Inverter Topology with Capacitor Voltage Self-Balancing

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ABSTRACT

In this paper, a novel six-level inverter is proposed. Voltage regulation is applied at DC-link and flying capacitors through the implementation of phase-shifted carrier-based modulation with zero-sequence voltage injection. The performance of the proposed structure has been verified under various modulation indices, where low voltage ripple is achieved at each capacitor and total harmonic distortions (THD) of line voltage at unity modulation index is about 15.95%.

1. Introduction

Over past several decades, multilevel converters have attracted wide attentions due to the numerous benefits which are offered, such as lower output voltage steps, reduced harmonic distortions, alleviated electromagnetic interference, and lower voltage stress at switching devices.

The widely recognized classical topologies, such as neutral-point clamped inverter (NPC) and flying-capacitor inverter (FCI), have been considered as key enablers to the invention of novel and more advanced topologies [1]. These recent converters have been developed to obtain optimum performance in various applications. Numerous advanced hybrid inverters have also been developed for DC-AC operation [2]-[4]. These topologies can be seen as derivations of active neutral-point clamped (ANPC) inverters, where one capacitor is added to the neutral point of DC-link. In comparison with the classical flying-capacitor inverter, these topologies require less flying-capacitor sub-circuits in order to obtain the same number of voltage level. However, these topologies require special balancing control to regulate the DC-link capacitor voltages and maintain all flying-capacitor voltages simultaneously. This requirement can be satisfied by either adding external balancing circuit or applying specific modulation techniques. In the former method, more passive and active components are needed, hence the device count is increased.

In this paper, a six-level hybrid flying-capacitor inverter (6L-HFCI) is proposed with capability of capacitor self-balancing. The regulation of all DC-link and flying-capacitor voltages are implemented through the injection of zero-sequence voltage to corresponding reference values. With the proposed topology, low total harmonic distortions (THD) can be achieved at line-to-line voltages. The effectiveness of the proposed structure and operating scheme is verified through simulation results.

2. Operating Principle of Six-Level Hybrid Flying-Capacitor Inverters

2.1 Configuration

The structure of three-phase 6L-HFCI is shown in Fig. 1. All of phase legs a, b, and c are fed from the same DC-link capacitor voltage at V_{dc}. If the base voltage is $E = V_{dc}/5$, the upper and lower capacitors voltages are set at E, whereas the middle capacitor voltage is set at $3E$. The voltage stress at each switching device is E.

Each phase in this structure requires three flying-capacitor units with different voltages. The values of capacitances and voltages between two capacitors at the same phase are inversely related. The benefit of employing capacitors which have the same voltage rating can also be obtained by configuring multiple capacitors in series for capacitors with higher voltage, hence the lower equivalent capacitance.

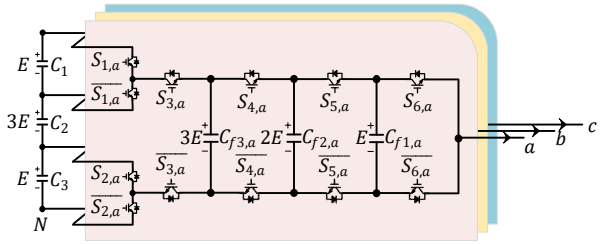

Fig. 1. Configuration of three-phase 6L-HFCI.

TABLE I. COMPARISON OF SIX-LEVEL INVERTERS

Topologies	Number of Capacitors		Number of Active Switches	Number of Clamp Diodes
	Base Voltage	Different Units		
6L-FCI	35	13	30	0
6L-NPC	5	5	30	24
6L-HI	11	6	36	0
6L-HFCI	23	12	36	0

Unlike the predecessor topology called 6L-HI, the proposed 6L-HFCI does not require any external DC-link balancing circuit [4]. When uniformity of devices is prioritized, this topology also demands lower device quantity compared to 6L-NPC and 6L-FCI, as listed in Table I.

2.2 Operating Principle

The selection of switching states and modulation technique should consider the operation with dead-time effect, which can cause undesirable multiple voltage steps. When phase-shifted carrier-based modulation (PS-PWM) is employed, such phenomenon can be avoided since only one gating signal is changed at every switching event. Therefore, dead-time only causes a slight delay at the output voltage.

Under ideal PS-PWM modulation, the reference waveform ($v_{ref,x}$) is compared with five fixed carrier waves, each of which is shifted 72° from each other. Meanwhile, the output voltage level can be expressed as:

$$v_{xN} = (S_{1,x} + S_{3,x} + S_{4,x} + S_{5,x} + S_{6,x})E, \quad (1)$$

where v_{xN} represents output phase voltage as a function of the switching states in the corresponding phase leg. Note that $S_{1,x}$ is equal to $S_{2,x}$.

If duty ratios of the aforementioned switches are defined as $d_{1,x}$, $d_{2,x}$, $d_{3,x}$, $d_{4,x}$, $d_{5,x}$, and $d_{6,x}$, respectively, the average output phase voltage over a span of carrier period can be obtained as:

$$u_x = (d_{1,x} + d_{3,x} + d_{4,x} + d_{5,x} + d_{6,x})E = d_{sum,x}E. \quad (2)$$

In an ideal PS-PWM scheme, where all capacitors voltages are assumed to be balanced, all duty ratios can be considered as constant in a carrier period as follows:

$$d_{sum,x} = 5v_{ref,x}. \quad (3)$$

To maintain all capacitors voltages, the currents that flow through neutral points and each flying capacitor are controlled by regulating the duty ratio of nearest switches. This control is illustrated in Fig. 2, where zero-sequence voltages (ZSV) are injected to the reference waveform and

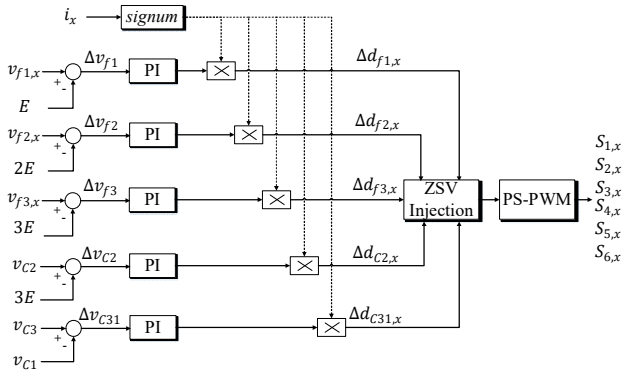

Fig. 2. Control of DC-link and flying-capacitors voltages.

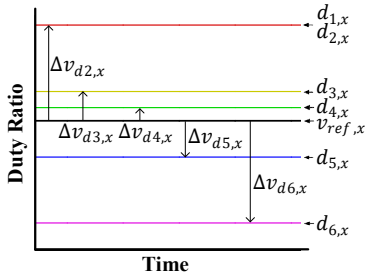

Fig. 3. Adjustment of duty ratio with zero-sequence voltage injection for capacitor voltages balancing.

implemented through the following equations:

$$\Delta v_{d2,x} = -\frac{\Delta d_{f1,x}}{4} - \frac{\Delta d_{f2,x}}{3} - \frac{\Delta d_{f3,x}}{2} - \Delta d_{C2,x} + \Delta d_{C31,x}, \quad (4)$$

$$\Delta v_{d3,x} = -\frac{\Delta d_{f1,x}}{4} - \frac{\Delta d_{f2,x}}{3} - \frac{\Delta d_{f3,x}}{2} + \frac{\Delta d_{C2,x}}{4} - \Delta d_{C31,x}, \quad (5)$$

$$\Delta v_{d4,x} = -\frac{\Delta d_{f1,x}}{4} - \frac{\Delta d_{f2,x}}{3} + \frac{\Delta d_{f3,x}}{3} + \frac{\Delta d_{C2,x}}{4}, \quad (6)$$

$$\Delta v_{d5,x} = -\frac{\Delta d_{f1,x}}{4} + \frac{\Delta d_{f2,x}}{2} + \frac{\Delta d_{f3,x}}{3} + \frac{\Delta d_{C2,x}}{4}, \quad (7)$$

$$\Delta v_{d6,x} = \Delta d_{f1,x} + \frac{\Delta d_{f2,x}}{2} + \frac{\Delta d_{f3,x}}{3} + \frac{\Delta d_{C2,x}}{4}, \quad (8)$$

$$d_{n,x} = v_{ref,x} + \Delta v_{dn,x} \quad (n = 2, \cdots, 6). \quad (9)$$

This ZSV injection causes divergence at switches duty ratios as illustrated in Fig. 3. Note that the summation of all ZSV components given in (4)-(8) should be equal to zero in order to maintain the same output voltage as that of the initial reference, which can be written as follows:

$$\begin{cases} d_{sum,x} = 5v_{ref,x} + \sum_{i=2}^{6} \Delta v_{di,x} \\ \sum_{i=2}^{6} \Delta v_{di,x} = 0 \end{cases}, \quad (10)$$

where the divergence effect on the output voltage is eliminated.

3. Simulation Results

In this section, simulations are performed for the operation of the 6L-HFCI, where the input DC voltage, fundamental frequency, and switching frequency are 7000 V, 60 Hz, and 2000 Hz, respectively. The capacitance of outermost, middle, and innermost flying capacitors are 2 mF, 1 mF, and 0.667 mF, respectively, whereas those of upper, middle, and lower DC-link capacitors are 2 mF, 0.667 mF, and 2 mF, respectively. The load resistance and inductance are 20 Ω and 6 mH, respectively.

The simulation results for pole and line voltages at both high and low amplitude modulation indices are shown in Fig. 4. All capacitor voltages are balanced at the reference values as shown in Fig. 5, where the proposed 6L-HFCI is operated at various modulation indices (m_a). The voltage ripple becomes even lower at lower m_a values.

The total harmonic distortions of line-to-line voltages at various amplitude modulation indices are shown in Fig. 6. Note that the values are almost identical for both high and low frequency modulation indices. At unity modulation index, the THD value is 15.95%.

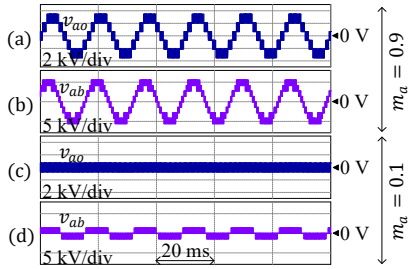

Fig. 4. Simulation results at $f_0 = 60\ Hz$. (a) Pole voltage at $m_a = 0.9$. (b) Line voltage at $m_a = 0.9$. (c) Pole voltage at $m_a = 0.1$. (d) Line voltage at $m_a = 0.1$.

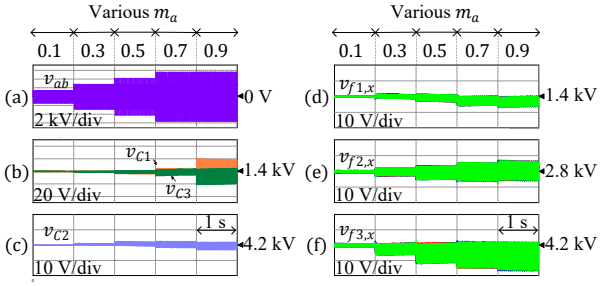

Fig. 5. Simulation results at various m_a and $f_0 = 60\ Hz$. (a) Line voltage. (b) DC-link capacitor voltages. (c) Middle DC-link capacitor voltage. (d) Outermost flying-capacitor voltages. (e) Middle flying-capacitor voltages. (f) Innermost flying-capacitor voltages.

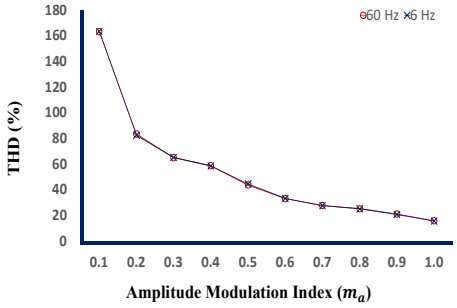

Fig. 6. Total harmonic distortions (THD) of line voltages at various m_a.

4. Conclusions

In this paper, a novel six-level hybrid flying-capacitor inverter (6L-HFCI) has been proposed. With competitive number of devices, this topology exhibits the capability of self-capacitor voltage balancing without requiring any auxiliary DC-link balancing circuit. The effectiveness of the proposed balancing algorithm has been verified through simulation results, where the THD value at unity modulation index is 15.95%.

References

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