4-레벨 하이브리드 하프 브리지 플라잉 캐패시터 인버터의 새로운 토폴로지

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A New Topology of Four-Level Hybrid Half-Bridge Flying-Capacitor Inverter

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ABSTRACT

This paper proposes the operation scheme and control method for a four-level hybrid half-bridge flying-capacitor inverter (4L-HHBFCI). With in-phase disposition level-shifted modulation (IPD), the flying capacitor voltage ripple is less than 1% of the reference value, while the line-to-line voltage total harmonic distortion is 23.27% at unity modulation index. The performance and effectiveness of the proposed inverter operation have been verified by simulation results.

1. Introduction

Multilevel voltage-source inverters (VSI) possess a number of traits that enable various applications to achieve better power quality. Under medium-voltage operation, the fluctuation of the pole voltage over the time (dv/dt) can be reduced by increasing the number of voltage level, and therefore decreasing the amplitude of voltage steps. Hence, the harmonic distortions can be reduced and the electromagnetic interference at the output voltages can be minimized.

A four-level hybrid-clamped (4L-HC) inverter has been developed for dc-ac operation [1]. As shown in Fig. 1(a), this topology is similar to a five-level Active Neutral-Point Clamped Inverter. It can be seen as the combination of two half-bridge sub-circuits and a three-level Flying-Capacitor Inverter (FCI). Other similar topologies also have been developed for higher level operation by adjusting the capacitors voltage distribution or adding more components [2], [3].

In this paper, a novel four-level hybrid half-bridge flying-capacitor (4L-HHBFCI) shown in Fig. 1(b) is proposed and operated under in-phase disposition (IPD) level-shifted PWM. This structure is equipped with the benefit of switching redundancy due to the connection of a half-bridge sub-circuit to the FCI sub-circuit, and thus provides the alternative conduction paths. Therefore, the appropriate switching state can be selected to maintain the flying-capacitor voltage by releasing a charging or discharging current. This regulation technique keeps the voltage near the reference value with a simple control function. The operation and performance of this inverter operation, including the harmonic profiles and the power losses at various modulation indices and different power factors, are validated by simulation results.

2. Operating Principle of Four-Level Hybrid Half-Bridge Flying-Capacitor Inverters

2.1 Configuration

The structure of the three-phase 4L-HHBFCI is shown in Fig. 2, where x represents each phase (either a, b, or c). These three legs share the common dc-link capacitors, where the upper and lower capacitors are rated at E and $2E$, respectively ($E = V_{dc}/3$). The voltage stress at $\overline{S_{2,x}}$ is $2E$, while each of the other switches only suffers E . The dc-link capacitors voltages are regulated by the auxiliary circuit, which can simply be a step-down dc-dc converter. Note that each flying capacitor should be regulated at $V_{dc}/3$.

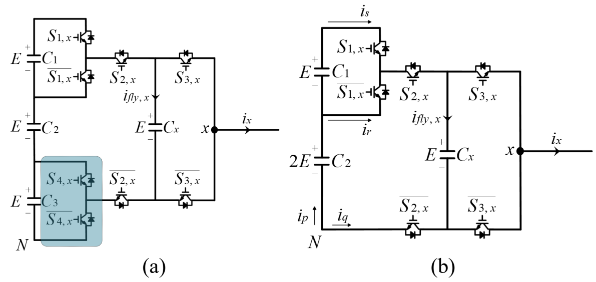


Fig. 1. Four-level inverters. (a) 4L-HC inverter [1]. (b) 4L-HHBFCI.

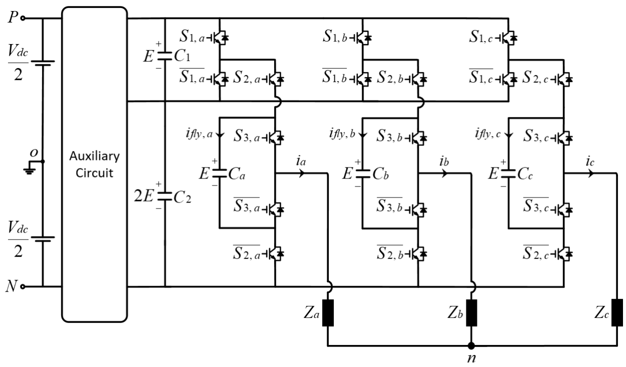


Fig. 2. Configuration of three-phase 4L-HHBFCI.

TABLE I. SWITCHING STATES OF 4L-HHBFCI

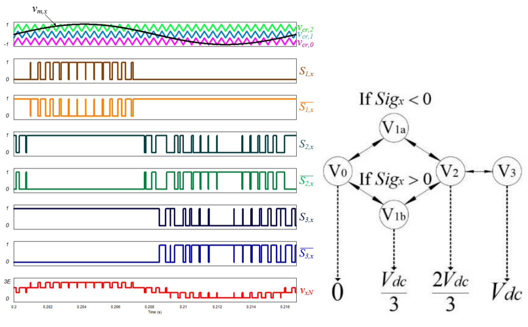
Switching States	Device Switching Status			v_{xN}	$i_{fly,x}$
	$S_{1,x}$	$S_{2,x}$	$S_{3,x}$		
V_0	0	0	0	0	0
V_{1a}	0	1	0	E	+
V_{1b}	0	0	1	E	-
V_2	0	1	1	$2E$	0
V_3	1	1	1	$3E$	0

2.2 Operating Principle

The switching states and device switching status for 4L-HHBFCI under IPD modulation are listed in Table I. The modulation waves ($v_{m,x}$) is compared with three fixed carrier waves ($v_{cr,0}$, $v_{cr,1}$, and $v_{cr,2}$) at a certain modulation index (MI) as shown in Fig. 3(a). Meanwhile, the output voltage level can be expressed as:

$$v_{xN} = [(S_{1,x})(S_{2,x}) + (S_{2,x} + S_{3,x})]E \ . \qquad (1)$$

The conduction path of the current that flows out of node N , either i_p or i_q , is driven by the switching status of $S_{2,x}$, regardless of the status of $S_{3,x}$.



(a) (b)

Fig. 3. Modulation technique for 4L-HHBFCI. (a) Gating signals with IPD modulation. (b) Switching states transition.

The output current i_x is determined by the instantaneous output phase voltage and load parameters. It also can be expressed as:

$$i_x = (S_{2,x})(i_p) + (1 - S_{2,x})(i_q) \ . \tag{2}$$

At the upper dc-link capacitor, both i_s and i_r flow according to the switching status of $S_{1,x}$ and $S_{2,x}$, which can be expressed as follows:

$$i_r = (1 - S_{1,x})(S_{2,x})(i_x) \tag{3}$$

$$i_s = (S_{1,x})(S_{2,x})(i_x) \ . \tag{4}$$

Meanwhile, the instantaneous flying-capacitor current can be expressed as follows:

$$i_{fly,x} = (S_{2,x} - S_{3,x})i_x \ . \tag{5}$$

The current can only flow through the flying-capacitor when these two switches have different gating signals. This enables the balancing of flying-capacitors voltages through the regulation of charging and discharging currents. A *signum* function is defined in (6) and used to select the switching state as shown in Fig. 3(b).

$$Sig_x = \text{sgn}[(v_{fc,x} - V_{dc}/3)i_x] \ . \tag{6}$$

The term Sig_x represents the status of capacitor voltage balance. It is specifically used to generate E at v_{xN}. If the value is negative, switching state V_{1a} should be selected, otherwise V_{1b} is selected. The other switching states do not contribute to the current that conducts through the flying capacitor, and thus give no effect to the voltage balance.

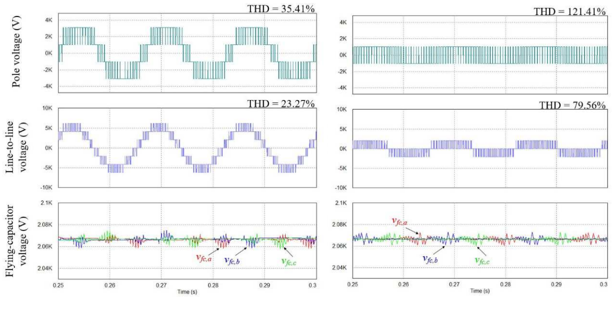
3. Simulation Results

In this section, simulations are performed for the operation of the 4L-HHBFCI, where the input dc voltage, fundamental frequency, and switching frequency are 6200 V, 60 Hz, and 2000 Hz, respectively. The dc-link capacitors are assumed to be controlled at the reference values. The capacitance of each flying capacitor is 2 mF, whereas the load resistance and inductance are 18.8 Ω and 6.6 mH, respectively.

Fig. 4 shows the output voltages at MI=1 and MI=0.3. At unity MI, the total harmonic distortions (THD) of the pole and line-to-line voltages are 35.41% and 23.27%, respectively. At MI=1, the peak-to-peak value of each flying-capacitor voltage ripple is less than 17 V, which is lower than 1% of the flying-capacitor voltage reference. The voltage ripple becomes even lower at low MIs.

Fig. 5 shows the power loss evaluation at various modulation indices with FF200R33KF2C dual-switch IGBT device (3300 V/200 A) [4]. The conduction and switching losses in the transistors are symbolized by $P_{cond,Q}$ and $P_{sw,Q}$, whereas those of the anti-parallel diodes are denoted as $P_{cond,D}$ and $P_{sw,D}$, respectively. The power losses at low MIs are lower due to the lower output currents and reduced conduction losses in the transistors and anti-parallel diodes.

The power losses at various displacement power factors (DPF) or $\cos(\phi)$ under constant impedance load and unity modulation index are shown in Fig. 6. This DPF variation does not significantly affect the power losses.



(a) (b)

Fig. 4. Output voltages of 4L-HHFBCI. (a) MI=1. (b) MI=0.3.

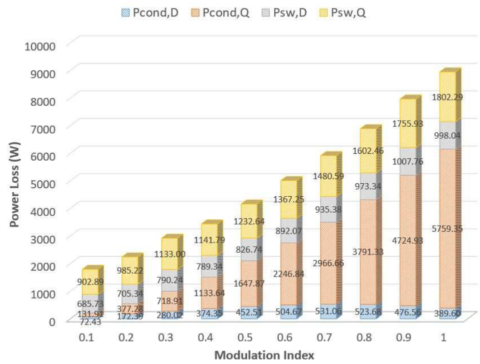


Fig. 5. Power losses at various modulation indices.

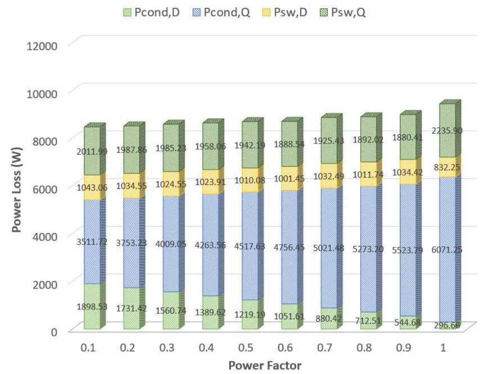


Fig. 6. Power losses at various displacement power factors.

4. Conclusions

In this paper, a four-level hybrid half-bridge flying-capacitor inverter (4L-HHBFCI) has been proposed along with the operating technique under in-phase disposition (IPD) level-shifted modulation. The THD values of the pole and line-to-line voltages at unity modulation index are 35.41% and 23.27%, respectively. The peak-to-peak value of each flying capacitor voltage ripple is less than 1% of the reference.

References

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