계통연계 인버터를 위한 새로운 고조파 보상법

A Novel Harmonic Compensation Technique for the Grid-Connected Inverters

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ABSTRACT

The output current of the Grid Connected Inverter (GCI) can be polluted with harmonics mainly due to i) dead time in switches, ii) non-linearity of switches, iii) grid harmonics, and iv) DC link fluctuation. Therefore, it is essential to design the robust Harmonic Compensation (HC) technique for the improvement of output current quality and fulfill the IEEE 1547 Total harmonics Distortion (THD) limit i.e. <5%. The conventional harmonic techniques often are complex in implementation due to their i) additional hardware needs, ii) complex structure, iii) difficulty in tuning of parameters, iv) current controller compatibility issues, and v) higher computational burden. In this paper, to eliminate the harmonics from the GCI output current, a novel Digital Lock-In Amplifier (DLA) based harmonic detection is proposed. The advantage of DLA is that it extracts the harmonic information accurately, which is further compensated by means of PI controller in feed forward manner. Moreover, the proposed HC method does not require additional hardware and it works with any current controller reference frame. To show the effectiveness of the proposed HC method a 5kW GCI prototype built in laboratory. The output current THD is achieved less than 5% even with 10% load, which is verified by simulation and experiment.

1. Introduction

Grid Connected Inverters (GCIs) have received great attention in recent years, due to their ability to inject power from renewable energy sources to the grid. However, the quality of output power degrades by i) the dead-time effects, resulting from employment of dead time, ii) the conduction voltage drops across the power switches. The effects on the output voltages are also of two types: the first one is linear distortion (reduced magnitude of the fundamental component); other is the harmonic distortion of the voltage and current waveforms (mainly appeared as increased content of odd harmonics i.e. third, fifth and seventh)., iii) The third source of distortion is due to grid harmonics which are already present in the grid due to extensive use of non-linear loads nowadays. These all factors in result led to increase the GCI current THD [1].

In order to ensure the controlled power flow of GCIs, current controller strategy plays an important role. However, the detrimental effect of low order harmonics cannot be eliminated by the typical current control techniques i.e. stationary and synchronous frame control. Owing to this fact, robust HC techniques are needed to ensure the overall THD of output current under the limits specified by the grid standards.

There has been considerable literature published in the area of harmonic compensation in both synchronous and stationary frame control. In [2] the resonant structure is used in synchronous DQ frame to compensate two harmonics simultaneously. However, this technique employs the resonant block in both D and Q axis separately. Moreover, extracting harmonics from the stationary or dc quantities will be inaccurate due to the use of SOGI block as an orthogonal signal generation (OSG) block which acts as a low pass and a band pass filter. Hence the extracted harmonics from the dc quantities are inaccurate.

Another effective approach is to use multiple rotating frames [3] to extract and compensate certain harmonics, however, this leads to a complex structure in the controller and a high computational burden. A similar technique is presented in [4] in which multiple rotating frames are nested within the main synchronous frame, however, multiple frames make the control structure complex and lead to a difficulty in implementation.

The other harmonic compensation method in the stationary frame is proposed in the [5], in this technique each resonant structure is tuned at the desired harmonic frequency to compensate it in stationary frame. However, in this technique the digitization error of the resonant structure introduces the tuning error hence steady-state error is inevitable in compensation and therefore the tuning process is complex.

Previous works for harmonic compensation in synchronous frames and stationary frames shows some drawbacks such as implementation complexity and increased computational burdens. In this paper Digital Lock-In Amplifier (DLA) based harmonic compensation technique is proposed. The proposed DLA based compensation technique is equipped with detecting not only amplitude but also the phase information of the selected harmonics, accurately. The proposed DLA HC algorithm has following advantages over the conventional methods, i) Proposed method does not require any additional hardware, it only require the current feedback information ii) DLA HC is independent of reference frame of current controller, iii)DLA HC control parameters are easy to tune because it contains only LPF and PI controller, iv) DLA HC is generalized, and it is capable of compensating any order of harmonic, v) It is immune to any kind of DC offset, high frequency noise and other measurements errors due to feedback sensor inaccuracies and vi) Proposed HC is independent of PLL phase angle. The working principle and design procedure of the proposed method will be explained in the next section.

2. The Proposed Harmonic Compensation Technique

In literature review, it has been realized that the main reason for the imperfect harmonic elimination by the previous approaches can be attributed to the inaccurate harmonic detection. In this paper Digital Lock-in Amplifier (DLA) based accurate and robust harmonic detection and elimination method is proposed. It is also known as phase-sensitive detectors, which are widely used in physical instrumentation for the extraction of

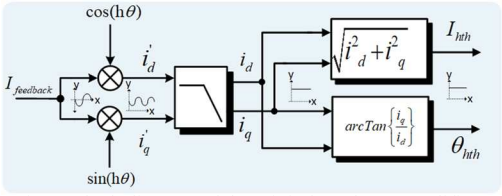


Fig. 1 Block diagram of the Digital Lock-In Amplifier

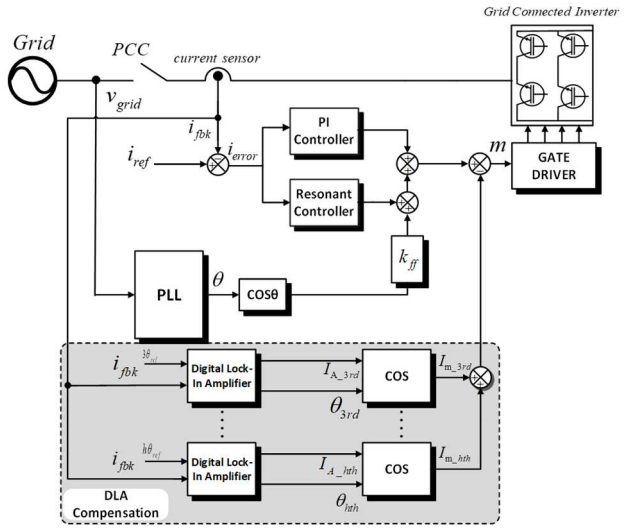


Fig. 2 Control structure of Single-Phase Grid Connected Inverter with proposed DLA harmonic compensation

low-level periodic signals buried in random noise and other disturbances. Fig. 1 shows the general structure of the DLA, it works on the principle of multiplying the input signal with the reference signal with a fixed frequency whose amplitude and phase information is required, Reference signals to extract 3rd, 5th and 7th harmonics are generated with the help of Digital Signal Processors (DSP) with an arbitrary phase. Multiplication of input signal yields the signal named as "Demodulator Outputs". Amplitude and phase of respective harmonics can be calculated through the demodulator outputs, which will be explain in following:

$$I_{feedback} = I_{amp}\begin{pmatrix}\cos(\omega_g t+\theta_g)+k_{3h}\cos(3\omega_g t+3\theta_g)\\ +\ldots+k_{nh}\cos(n\omega_g t+n\theta_g)\end{pmatrix} \quad (1)$$

Eq. (1) Show the characteristics equation of the single-phase inverter output feedback current which contains odd harmonics up to k^{th} order, where I_{amp} is the peak amplitude value of the fundamental 60Hz current component, where "k" is the amplitude of respective amplitude.

$$I_{d_{hth}} = I_{feedback} * I_{hth_{ref}} \Rightarrow I_{feedback} * \cos(h\omega_h t + h\theta_h)$$
$$I_{q_{hth}} = I_{feedback} * I_{hth_{ref}} \Rightarrow I_{feedback} * \sin(h\omega_h t + h\theta_h) \quad (2)$$

Eq. (2) shows the multiplication of the reference signals with current feedback signals. Multiplication of two sinusoidal signal yields two frequency components as an output i) DC component i.e. f-f_{ref} which contains amplitude and phase information of the desired harmonic, ii) double frequency component f+f_{ref} which is undesired and can be filtered with low pass filter at the output of the DLA.

$$I'_{d\_hth} = \frac{k_{nh}}{2}\left[\cos\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)\right] \quad (3)$$

$$I'_{q\_hth} = \frac{k_{nh}}{2}\left[\sin\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)\right] \quad (4)$$

Eq. (3) and (4) are the final demodulator outputs which contains the harmonics amplitude and phase information.

$$A_{hth} = \sqrt{\left(\frac{k_{nh}}{2}\right)^2\begin{Bmatrix}\left[\cos\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)\right]^2\\ +\left[\sin\left((h\omega_{PLL}-h\omega_g)t+(h\theta_{PLL}-h\theta_g)\right)\right]^2\end{Bmatrix}} \quad (5)$$

Pythagorean theorem is applied on Eq. (5) for further simplification to remove the sine and cosine terms, which yields the final amplitude of the desired harmonic in Eq. (6).

$$A_{hth} = \left(\frac{k_{nh}}{2}\right) \quad (6)$$

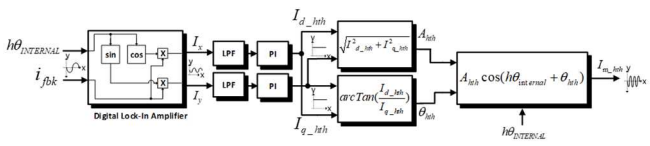


Fig. 3 h^{th} order DLA Harmonic Compensator block Diagram

In order to calculate phase difference between the reference signal and the harmonic signal phase, arctangent is applied on the PSD outputs Eq. (3) and (4), which yields the output in Eq. (7).

$$\theta_{hth} = Tan^{-1}\left\{\frac{\frac{k_{nh}}{2}\left[\sin\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)\right]}{\frac{k_{nh}}{2}\left[\cos\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)\right]}\right\} \quad (7)$$

The following equation can be obtained after some further simplification and normalization.

$$\theta_{hth} = \overbrace{\left((h\omega_{REF}-h\omega_g)t+(h\theta_{REF}-h\theta_g)\right)}^{\theta_{error}} \quad (8)$$

Eq. (8) is the relation where the phase error between the reference signal and the actual harmonic signal is shown.

Now the accurate amplitude and phase information of harmonic is extracted, exact replica of the any h^{th} harmonic can be regenerated using the relation shown in Eq. (8).

In proposed method, amplitude and phase of 3rd, 5th and 7th harmonic is extracted through DLA. Detailed block diagram of h^{th} order compensator is shown in Fig. 3. Harmonics are compensated with the simple PI controller, which is implemented after PSD, PI controller is used to remove harmonic steady state error. The output of the PI controller is used for cosine to regenerate the replica of the harmonic which is present in the inverter current output i.e. I_{m_hth}.

$$I_{m\_hth} = A_{hth\_PI}\cos(h\theta_{REF}+\theta_{hth}) \quad (8)$$

Eq. (8) shows the harmonic regeneration expression. This regenerated h^{th} order harmonic is compensated by subtracting it from the final modulation signal produced by the current controller in a feedforward manner.

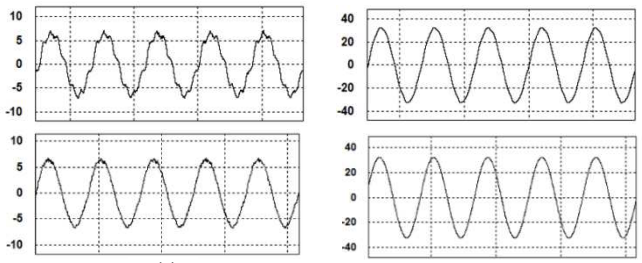
$$G_{ol_h}(s) = \left(\frac{\omega_c}{s+\omega_c}\right)^k \times \left(\frac{k_p s+k_i}{s}\right) \quad (9)$$

Eq. (9) shows the open loop gain of the DLA HC compensator. To achieve optimal dynamic and steady state performance PI is designed in SISO tool in MATLAB software. The parameters k_p and k_i are to be 1.489 and 12.07, for 3rd, 5th and 7th harmonic compensator, respectively.

3. Simulation and Experiment Results

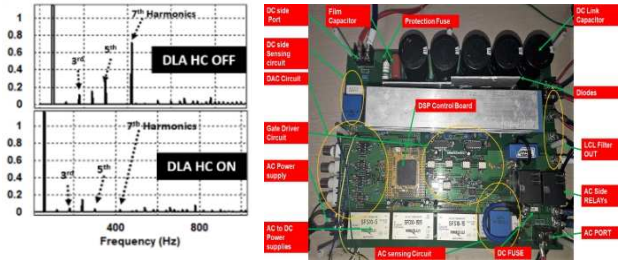
Simulations and experiments are carried out with a 5kW inverter to evaluate the performance of the proposed harmonic compensation method under the non-sinusoidal grid conditions. The specification of the inverter is given in Table I. Fig. 4 shows the simulation results at (a) 1kW and (b) 5kw. As shown in the figure, under the non- sinusoidal grid condition inverter output current is distorted with THD of 11.52% and 2.55% at 1kW and 5kW respectively. However, when 3rd, 5th and 7th harmonic is compensated by the proposed DLA Harmonic compensator, THD is reduced to 4.56% and 0.93% at 1kW and 5kW respectively. Fig. 5(a) shows the FFT of inverter current at 1kW with and without DLA compensator, difference in performance is clearly visible, harmonics are removed completely.

Fig. 5(b) shows the 5kW inverter circuit used for the experiment in a grid connected mode. Fig. 6 shows the experimental results for 1kW and 5kW. It is shown that THD at



(a) (b)

Fig. 4 Simulation Results with and without HC at (a) 1kW (b) 5kW



(a) (b)

Fig. 5 Experiment results at different load conditions with non-sinusoidal grid condition (a) FFT with and without compensation (b) 5kW Inverter Prototype used for the experiments

1kW is reduced from 25.7% to 4.77%, whereas at full power THD is reduced from 8.36% to 1.58%. In Table II the results at other power are summarized. Table IV shows that THD at all the powers without any compensation was way above than the allowed 5% threshold. With DLA HC enabled, Inverter under distorted grid conditions is able to achieve less than 5% THD for entire load range.

TABLE I
SYSTEM PARAMETERS FOR SIMULATION AND EXPERIMENTAL RESULTS

Parameters		Values
Grid Voltage THD	THD	3.49%
Rated Power	P_o	5kW
Switching Frequency	f_{sw}	10kHz
Dead time	t_d	0.5µs
Inverter side inductor	L_i	1.4mH
Grid side inductor	L_g	1.2mH
Filter capacitor	C_f	6.0µF

It can be realized from the TABLE II that proposed method improves the THD in inverter output current for load range between 10% to 100% rated power. Moreover, computational time of overall harmonic compensation loop employed for 3rd, 5th and 7th harmonics combined was measured as 16uS in TMS320F28335F Digital Signal Processor.

TABLE II
THD TABLE WITH AND WITHOUT DLA COMPENSATION

POWER	Without HC	With DLA HC	% Harmonic Reduction
1 KW	25.71%	4.77%	97%
2 KW	13.54%	2.73%	94.3%
3 KW	10.49%	2.23 %	91%
4 KW	8.74%	1.73%	89%
5 KW	8.36%	1.58 %	86.5%

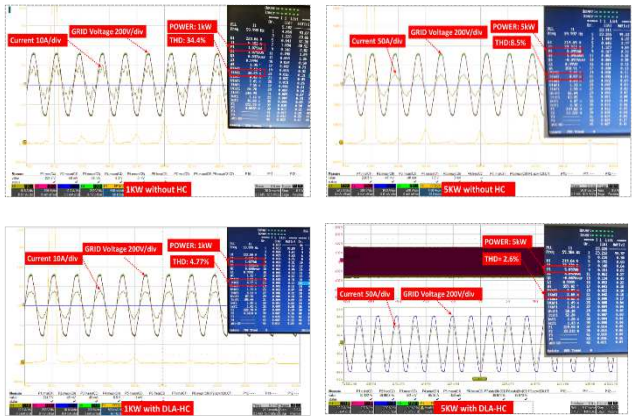


Fig. 6 Experiment Results at different Load conditions with non-sinusoidal grid. (a) 1kW test without HC (b) 1kW test with DLA HC enabled (c) 5kW test without HC (d) 5kW test with DLA HC enabled

4. Conclusion

This paper proposed a simple but cost-effective inverter-current harmonic mitigation strategy for the grid connected inverters based on Digital Lock-In Amplifier (DLA) to achieve multiple harmonic compensation. DLA HC works on the principle of frequency shifting/demodulation principle, amplitude and phase information any h^{th} order harmonic can be extracted and compensated accurately from the highly distorted feedback current signal. The DLA-HC ensured less than 5% THD for the 5kW grid connected inverter prototype for 10% to 100% rated power. The quality of inverter current for whole load range can be guaranteed even when the grid voltage is not ideal and severely distorted. Simulation and experimental results prove the efficacy of the proposed compensation technique with a significant reduction in THD.

REFERENCES

[1] R. Wang et al., "Harmonic compensation method using single-phase cascaded H-bridge converters," in The Journal of Engineering, vol. 2019, no. 16, pp. 1589-1593, 3 2019.

[2] M.Lisrerre, R. Teodorescu, F. Blaabjerg, "Multiple harmonic control for three phase grid converter system with the use of PI-RES current controller in rotating frame", IEEE Trans. Power Electron., Vol. 21, no. 3, May 2006.

[3] Castilla, M.; Miret, J.; Camacho, A.; Matas, J.; de Vicuna, L.G., "Reduction of Current Harmonic Distortion in Three-Phase Grid Connected Photovoltaic Inverters via Resonant Current Control,"

[4] David Campos-Gaona, Rafael Pena-Alzola, Jose Luis Monroy-Morales, Martin Ordonez, Olimpo Anaya-Lara, and William E.Leithead "Fast Selective Harmonic Mitigation in Multifunctionla Inverters Using Internal Model Controllers and Synchronous Reference Frame".IEEE Trans. Ind. Electron., , Vol. 64, no. 8, Aug. 2017.

[5] A. Maknouninejad, M. G. Simoes and M. Zolot, "Single phase and three phase P+Resonant based grid connected inverters with reactive power and harmonic compensation capabilities," 2009 IEEE International Electric Machines and Drives Conference, Miami, FL, 2009, pp. 385-391.