Optimal Design for Dynamic Resistance Equalization Technique to Minimize Power Loss and Equalization Error

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ABSTRACT

Dynamic resistance equalization is a viable technique to balance SOC of cells in a parallel-connected battery configuration due to high equalization performance, simplicity and low-cost. However, an inappropriate design of the equalization resistor can degrade the equalization performance and increase the power loss. This paper proposes an optimization process to design the equalization resistors to minimize power loss and equalization error. The simulation results show that the optimally designed resistor significantly enhance the performance in comparison with the conventional fixed-resistor equalization.

Keyword: parallel-connected battery, battery cell equalization, dynamic resistance equalizer.

1. INTRODUCTION

In demand to extend operation time in the long-term application as electric vehicles or reconfigurable battery storage system, multiple battery cells are connected in parallel [1]. While various equalization techniques for series-connected battery cells are reported in [2], just a few studies about battery equalization for parallel-connected battery have been done. Conventionally, battery cells with similar impedance are connected directly and rely on the self-balancing ability of parallel connection. Thus, the cell inconsistency still exists and cause the uncontrollable current sharing issue between parallel branches [3].

Fortunately, a viable technique based on dynamic resistance equalization method is introduced in [4] to maximize the battery capacity utilizing. The equalizer circuit is illustrated in Fig. 1 where each battery branch is connected to two power resistor and one switch to control the branch impedance. Based on the SOC rate of cells, the corresponding switch of highest SOC cell (in charging mode) or lowest SOC cell (in discharging mode) is turned off during the other switches are turned on. As a result, the load or charging current are shared with a designed ratio to equalize the SOC of cells. With a simple control scheme and low-cost, the dynamic resistance equalizer is promising for real application.

However, an inappropriate design of equalization resistor R_1 and R_2 can decrease the equalization performance, increase power loss and charge/discharge battery with a higher current that it can. This paper is an extension of [4] in order to provide guidance for the optimal resistance on equalizer circuit design. This paper introduces the operation principle of the equalization with power loss calculation in section 2, simulation results are performed in section 3 and the solution is made in section 4.

2. PROPOSED METHOD

To analyze the power loss on the equalizer circuit, a simulation of four parallel-connected battery in discharging mode is used as a case study. The modeling of the equalizer is shown in Fig. 2 where the impedance of parallel branches can be reconfigured by controlling the corresponding switches of battery. The equalization process is divided into 3 intervals

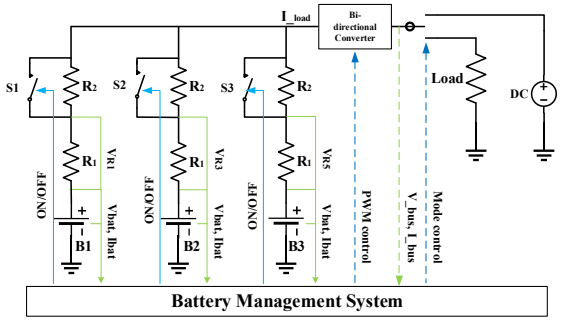

Figure 1: Dynamic resistance equalizer architecture [4]

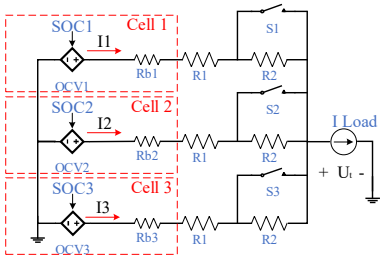

Figure 2: The modeling of the equalizer.

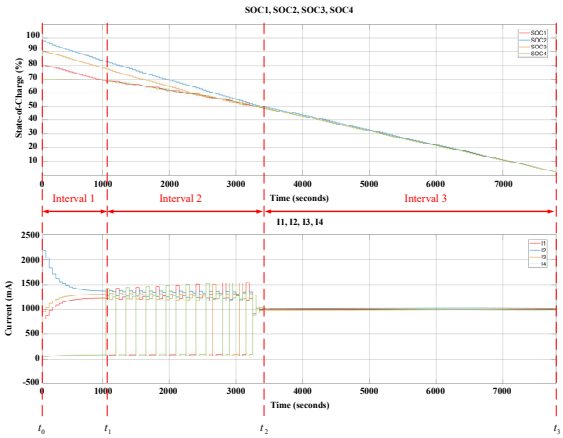

Figure 3: Battery SOC and current in discharging mode

(Fig. 3): interval 1 – base run equalization ($t_0 \rightarrow t_1$), interval 2 – sequentially switching ($t_1 \rightarrow t_2$) and interval 3 – cooldown equalization ($t_2 \rightarrow t_3$).

In the base run interval, load demand is shared unequally with a designed ratio to equalize the SOC of the lowest cell to the next higher cell. In this case study, assume that the battery cells have a similar capacity but different in initial SOC rate ($SOC_1 > SOC_3 > SOC_2 > SOC_4$. The switches in branch #1, #2, #3 are turned on and the switch in branch #4 is turned off. The impedances of each branch are calculated by (1), (2), (3) and (4), respectively.

$$Z_1 = Z_{on} = R_{b1} + R_1 + \frac{R_{d\_on}R_2}{\left(R_{d\_on} + R_2\right)} \quad (1)$$

$$Z_2 = Z_{on} = R_{b2} + R_1 + \frac{R_{d\_on}R_2}{\left(R_{d\_on} + R_2\right)} \quad (2)$$

$$Z_3 = Z_{on} = R_{b3} + R_1 + \frac{R_{d\_on}R_2}{\left(R_{d\_on} + R_2\right)} \quad (3)$$

$$Z_4 = Z_{off} = R_{b1} + R_1 + R_2 \quad (4)$$

By applying Kirchhoff law to the modeling in Fig. 2, the individual branch currents are obtained as (5).

$$\begin{aligned} Z_1 I_1 - Z_2 I_2 &= OCV_1 - OCV_2 \\ Z_1 I_1 - Z_3 I_3 &= OCV_1 - OCV_3 \\ Z_1 I_1 - Z_2 I_2 &= OCV_1 - OCV_4 \\ I_1 + I_2 + I_3 + I_4 &= I_0 \end{aligned} \quad (5)$$

Due to the changing on the SOC rate of cells, the equalization process is divided into multiple small-time step T. The changing on SOC is represented by equal (6) with Q is the capacity of the battery, I_i is the branches currents and SOC_i are the SOC of cells. With each combination of R_1 and R_2, at the process start t_0, the branches currents are different as Fig. 4. It is clear that the current sharing ratio is decided by R_2, and the value of R_2 can be decided to protect the battery from overload or maintain efficiency [5]. Assume that the initial SOC of cells are $SOC_{init1,2,3,4} = 100, 80, 90, 70\%$ of 2.6Ah capacity; the impedance of battery, R_b, is less than 70mΩ (datasheet of 186350 battery [6]); the load demand is constantly 4A. The chosen resistor R_2 is 500mΩ to maintain the maximum current of the battery cell is 0.75C.

Interval 1 is ended when the SOC of the lowest cell is equalized with the next higher SOC cell. Thus, the time point t_1 is calculated by (7), the average value of total conduction loss on the equalizer circuit is calculated by (8) with $P_i(k) = Z_i I_i(k-1)$ is the power loss of individual branch at each step k.

$$SOC_i(k) = SOC_i(k-1) - \frac{T.I_i(k-1)}{Q} \quad (6)$$

$$t_1 = kT \quad (7)$$

$$P_{int1\_ave} = \frac{T\sum P_i(k)}{t_1} \quad (8)$$

In interval 2, the switch in the highest SOC branch is turned on while the other branches are sequentially switching as the theoretical waveform in Fig. 5. With the assumption that cell #1 still is the highest SOC, the average current of cell #2, #3 and #4

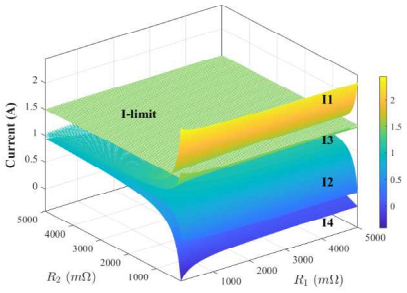

Figure 4: Current sharing ratio of branches with various R_1, R_2.

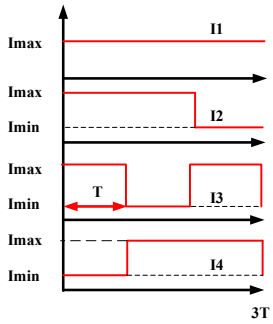

Figure 5: Theoretical waveform of battery currents in interval 2.

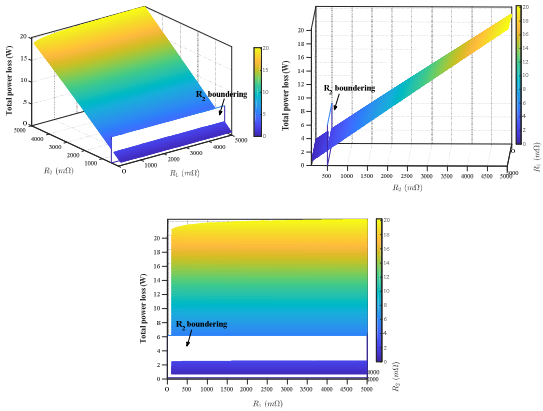

Figure 6: The average total conduction loss of equalizer circuit with various R_1, R_2.

is calculated by (9). The interval 2 is ended when the SOC of all cells are equalized and the approximate time point t_2 is calculated by (10), the power loss on branch #1 is calculated by (11) and the other branches are calculated by (12), with $I_{highest} = I_{max}$ and I_{min} is the current of branches at t_1.

$$I_{ave} = \frac{2I_{max} - I_{min}}{3} \quad (9)$$

$$t_2 = Q\frac{SOC_{highest}(t_1) - SOC_{lowest}(t_1)}{I_{highest} - I_{ave}} + t_1 \quad (10)$$

$$P_{1\_int2} = Z_{on} I_{max}^2 \quad (11)$$

$$P_{2\_int2} = P_{3\_int2} = P_{4\_int2} = \frac{2Z_{on} I_{max}^2 T + Z_{off} I_{min}^2 T}{3T} \quad (12)$$

In interval 3, the SOC of all cells are equalized. Assume that the battery capacity is fully utilized, the process end time point, t3, is calculated by (13). All switches are turned on to contribute equally to the load current with the lowest power loss. The current of branches in interval 3 is calculated by (14) and the power loss on branches is calculated by (15).

$$t_3 = Q\frac{\sum_1^N SOC_{i\_init}}{I_0} \quad (13)$$

$$I_{int3} = \frac{I_0}{N} \quad (14)$$

$$P_{1\_int3} = P_{2\_int3} = P_{3\_int3} = P_{4\_int3} = Z_{on} I_{int3}^2 \quad (15)$$

$$P_{loss} = \frac{P_{int1} t_1 + P_{int2}(t_2 - t_1) + P_{int3}(t_3 - t_2)}{t_3} \quad (16)$$

The average conduction loss of the whole equalization process is calculated by (16). With various value of R_1 and R_2,

the average total conduction loss of the equalizer circuit is shown in Fig. 6. With the chosen value of R_2 at t_0, the value of resistor R_1 is obtained to minimize the power loss of the system. With the case study, the chosen combination is $R_1 = 100m\Omega \; and \; R_2 = 500m\Omega$.

3. VERIFICATION OF THE PROPOSED METHOD

To verify the proposed method, a simulation for four parallel-connected 18650 battery cells (3.7V/2.6Ah) has been implemented in Matlab/Simulink. The battery system is working in discharging mode with load demand constant 4A. The equalization resistors and initial SOC of battery are set as the Table I with 3 different scenarios. The simulation results are shown in Fig. 7 and Fig. 8, respectively.

According to Fig. 7(a) and 8(a), resistor R_1 in scenario 1 is much larger than R_2, the load demand is contributed equally by branches and the SOC of cells is un-equalized. After 7000 seconds, cell #4 is fully discharged and the current of the other branches is increased. For both scenarios 1 and 2, the current sharing follows the algorithm of the dynamic resistance equalization (Fig. 8(b) and 8(c)). The current of branch #4 in scenario 3 is lower than scenario 2 which decrease the equalization time. The SOC profile in Fig. 7(b) and 7(c) show that the required times to equalize all cells in scenario 2 and 3 are 4300 and 3800 seconds, respectively. It means that the equalization speed is increased when the value of resistor R_2 is increased.

The comparison of the average total conduction loss in all branches is summarized in Table I. Although the design in scenario 3 has higher equalization speed than scenario 2, the power loss in scenario 3 is 18% higher. Thus, the design in scenario 2 is optimization in view of power loss.

Table I: Initial simulation condition and power loss comparison

	Scenario 1	Scenario 2	Scenario 3
$SOC_{init1,2,3,4}$	100, 80, 90, 70%		
Load demand	CC - 4A		
R1 & R2	1Ω & 0.1Ω	0.1Ω & 0.5Ω	0.1Ω & 1Ω
P_{loss} (W)	4.2	0.56	0.66

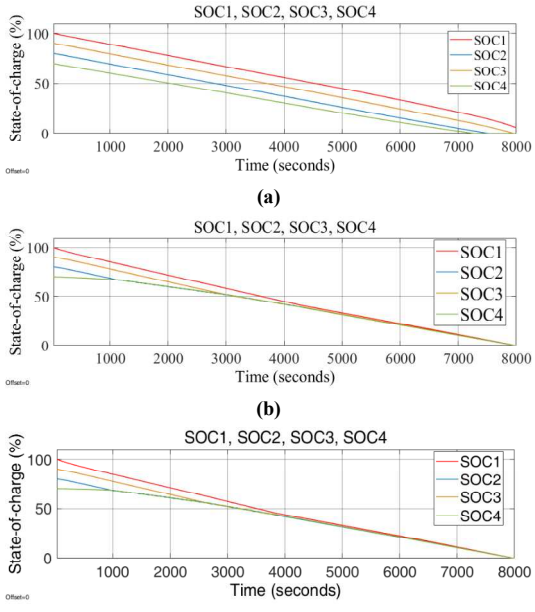

Figure 7: Battery SOC: (a) scenario 1; (b) scenario 2; (c) scenario 3.

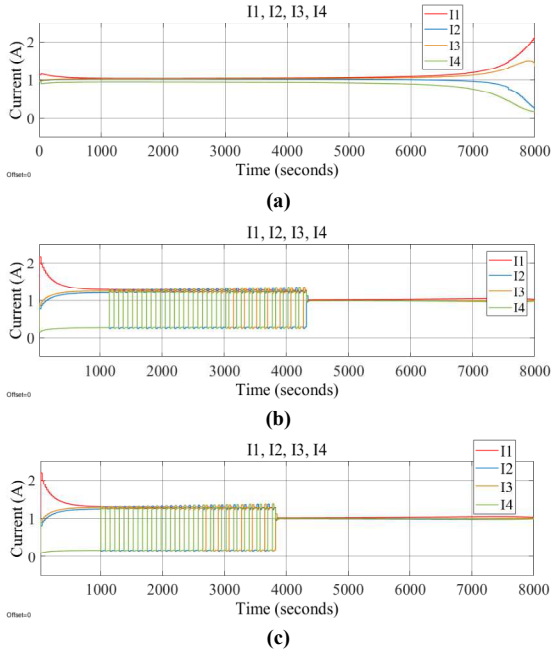

Figure 8: Battery current: (a) scenario 1; (b) scenario 2; (c) scenario 3.

4. CONCLUSION

This paper proposes to provide guidance to design the equalization resistor in dynamic resistance equalizer. Besides, the power losses in branches are analyzed individually in each interval. The simulation shows that the designed resistor can maximally utilize fully battery capacity and the branches current is confined in safety range with lowest conduction loss.

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