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NCP51705 Fully Integrated Low Side SiC Driver

Technical Presentation
Jan-2018

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NCP51705 – 6A SiC MOSFET Fully integrated Gate Driver

Value Proposition

The NCP51705 driver is designed to primarily drive SiC MOSFET transistors. For the lowest possible conduction losses, the driver is capable to deliver the maximum allowable gate voltage to the SiC MOSFET device. For improved reliability, dV/dt immunity and even faster turnoff, the NCP51705 can utilize its on-board charge pump to generate a user selectable negative voltage rail.

Unique Features

- **Adjustable, on-board regulated negative charge pump**
- Negative voltage drive for fast turn-off (same as above)
- 5V Reference/Bias Rail
- Adjustable UVLO levels

Benefits

- **Simplified BOM and no need for extra DC/DC**
- Easy digital isolator Vcc supply
- Can work with diff SiC FET's

Other Features

- High peak output current – 6A
- Extended positive voltage rating for efficient SiC MOSFET operation during the conduction period
- Thermal shutdown funct on
- DESAT detection for short circuit protection
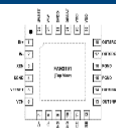- Inverting/Non-inverting Input

Market & Applications

- Industrial Inverters, Motor drives
- High Performance PFC, AC/DC & DC/DC Converters

Typical Application Schematic
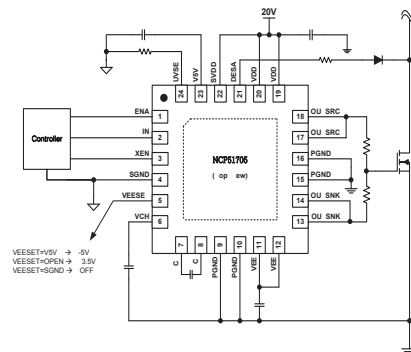

Ordering & Package information

- QFN24 4mm x 4mm
- OPN : NCP51705MNTXG

NCP51705 Pin Descriptions

- ➢ IN+; IN- – Non-Inverting and Inverting PWM inputs
  - • Low power mode is initiated when IN+ = LO & IN- = HI
- ➢ XEN – Output Status; Fault detection
- ➢ SGND – signal ground
- ➢ VEESET – negative bias level programming pin
- ➢ VCH – Charge pump supply voltage (bypass only)
- ➢ C+; C- – charge pump flying capacitor connections
- ➢ PGND – power ground; source of the SiC MOSFET
- ➢ VEE – bypass capacitor for the negative bias rail
- ➢ OUTSRC; OUTSNK – gate drive output pins
- ➢ VDD – device supply rail; defines positive gate drive amplitude
- ➢ SVDD - device supply rail; quiet rail for driver logic
- ➢ DESAT/CS – desaturation detection/current sense input
- ➢ V5V – controller low voltage bias; can power digital isolator
- ➢ UVSET – set UVLO turn-on threshold; sets minimum positive drive amplitude
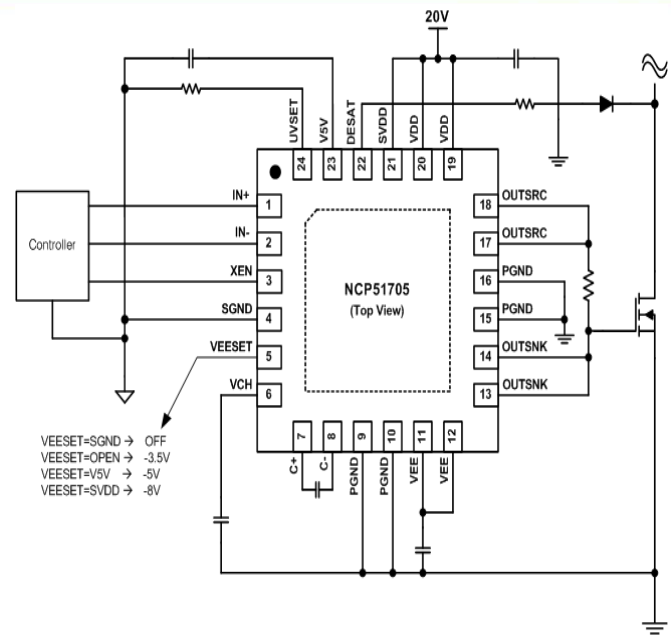
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NCP51705 Block Diagram

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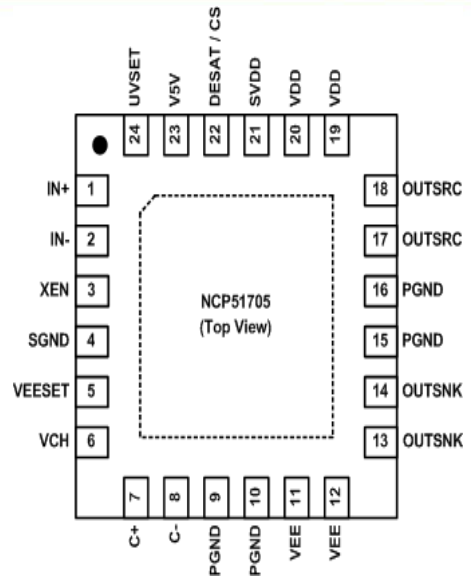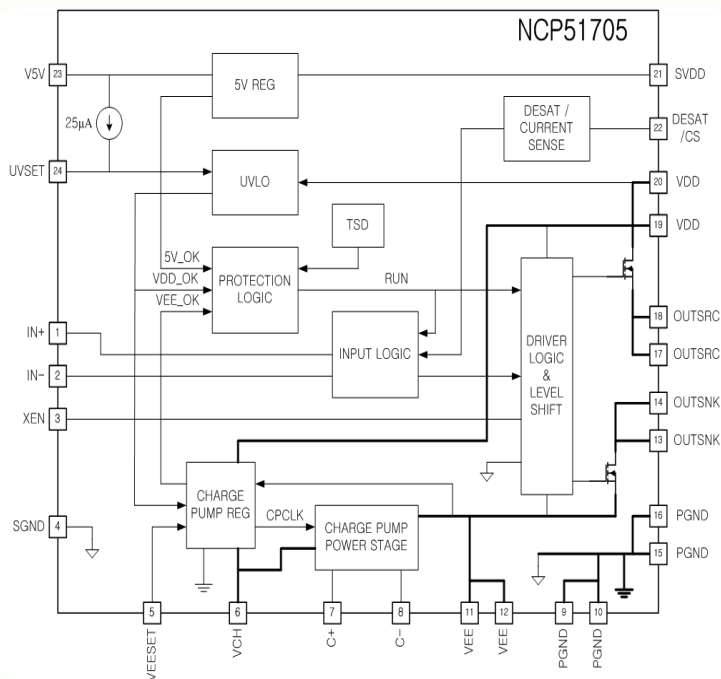
NCP51705 Driver Implementation – UVLO

- VDD and VDDS must be approximately the same voltage
  - A small value resistor and local bypass capacitor at VDDS can be used to ensure a quiet VDDS
- External 5V regulator follows VDD
- All voltage rails (VDD; V5V; VEE) are independently monitored
- $VDD_{(MIN)}$ =~8V; device is fully functional
  - Charge pump starts at $VDD_{(MIN)}$
- User programmable START threshold to ensure sufficient V_{GS} amplitude
  - START threshold is resistor programmable at UVSET pin


```
VEESET=SGND  →  OFF
VEESET=OPEN  →  -3.5V
VEESET=V5V   →  -5V
VEESET=SVDD  →  -8V
```
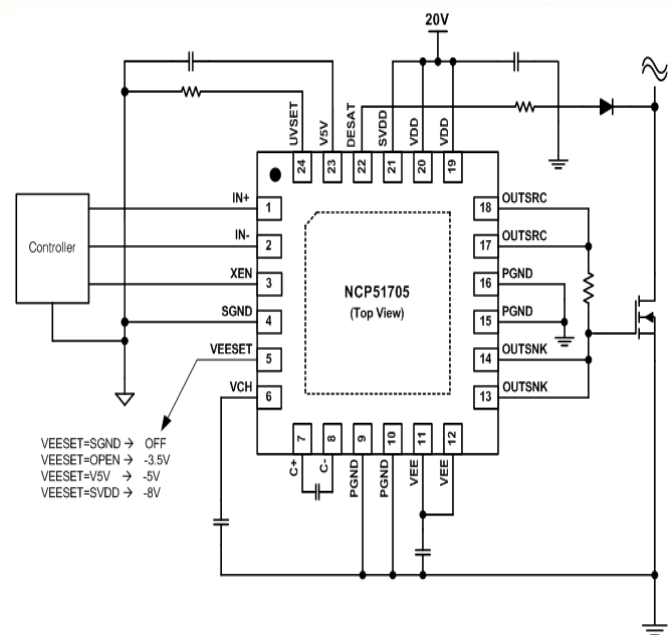
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NCP51705 Driver – Thermal Considerations

- User programmable START voltage has a great impact on SiC MOSFET power dissipation:
  - CREE C2M0080120 @20A; @25C°
  - $V_{(START)}$ =14V; RDSON=~270mΩ
  - $V_{(START)}$ =18V; RDSON=~90mΩ
  - P_{COND} is about 3 times higher @14V!
- START voltage has a fixed 1V hysteresis
  - Minimum operating voltage ($V_{(START)}$ – 1V) determines worst case thermal conditions


```
VEESET=SGND  →  OFF
VEESET=OPEN  →  -3.5V
VEESET=V5V   →  -5V
VEESET=SVDD  →  -8V
```

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NCP51705 Driver – Thermal Considerations

➢ NCP51705 has four major power loss sources:
  - Output stage losses associated to driving the external SiC MOSFET
  - Linear regulator between VDD and V5V output – external load
  - Linear regulator between VDD and VCH output
  - Charge pump switches

➢ If thermally limited, disable charge pump and use external negative bias

➢ NCP51705 has a thermally enhanced package:
  - **Bottom pad is not PGND!**

VEESET=SGND → OFF
VEESET=OPEN → -3.5V
VEESET=V5V → -5V
VEESET=SVDD → -8V

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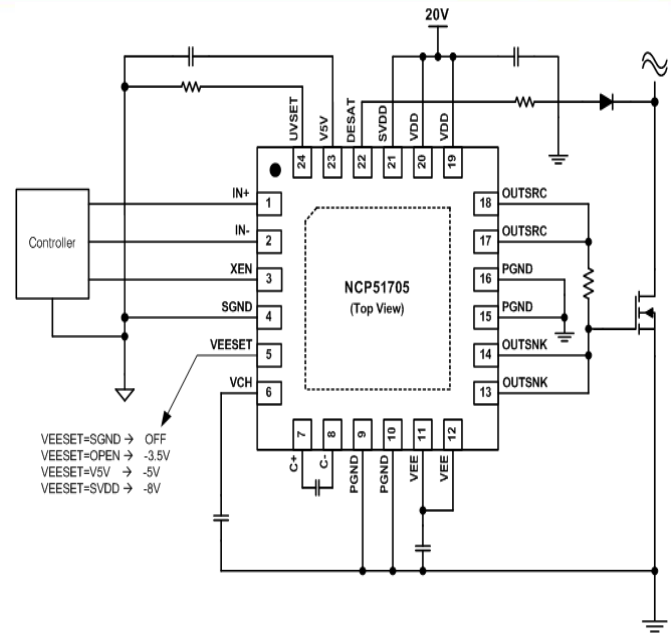
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NCP51705 Driver Implementation – VEE

➢ NCP51705 has an inverting, regulating charge pump:
  - VEE is independent of load
  - Fully integrated switches
  - Discrete steps adjustable VEE
    - V_{VEESET}=SGND; charge pump is disabled; VEE pins must be connected to PGND
    - V_{VEESET}=N/C (floating) VEE = -3V;
    - V_{VEESET}=V5V; VEE = -5V;
    - V_{VEESET}=SVDD; VEE = -8V

➢ When the charge pump is disabled the driver power dissipation is greatly reduced → helps at high frequency

VEESET=SGND → OFF
VEESET=OPEN → -3.5V
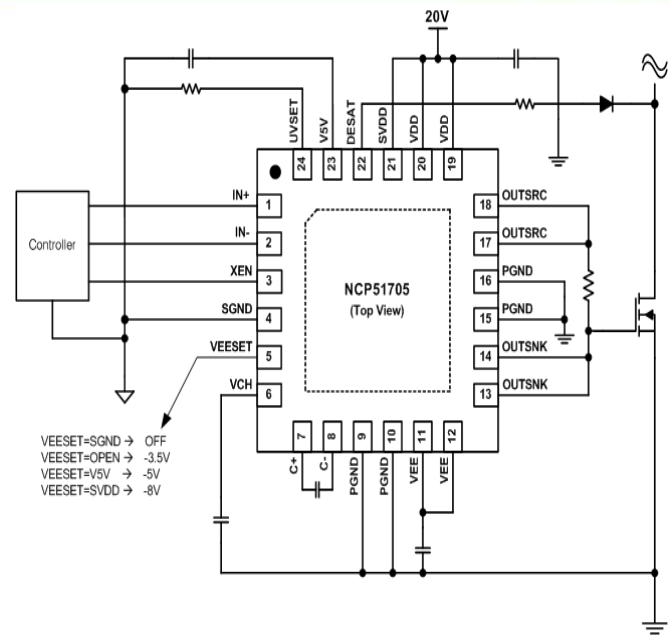VEESET=V5V → -5V
VEESET=SVDD → -8V
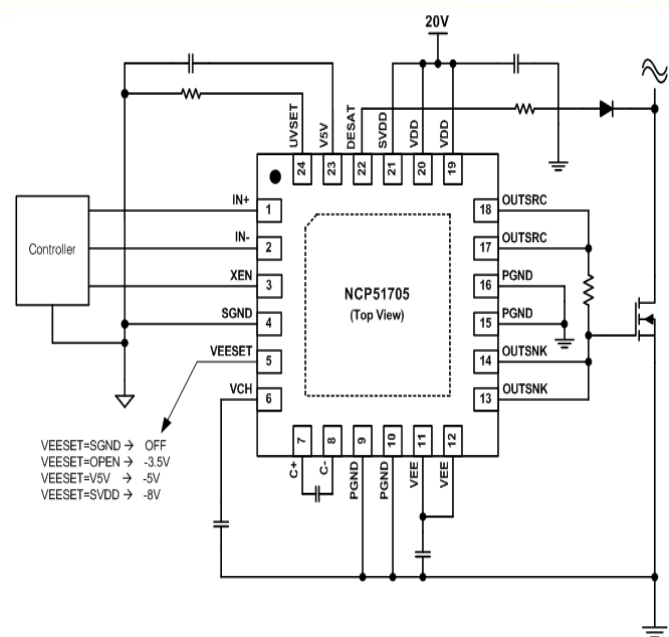
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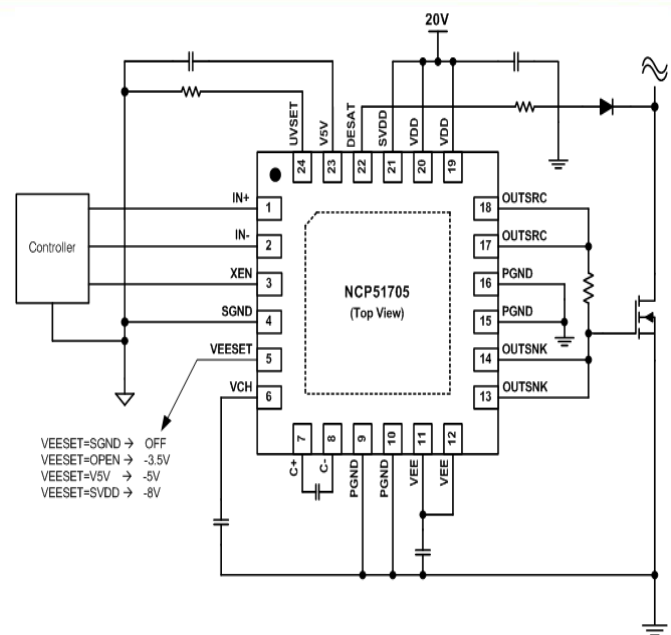
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NCP51705 Driver Implementation – Logic

- NCP51705 can be used as an inverting or as a non-inverting driver:
  - IN+ is the non-inverting input
  - IN− is the inverting input
- Both inputs are preset to OFF state by an internal resistor (100kΩ)
- When both inputs are inactive, low power mode is initiated (I_{DD} < 2mA)
  - Charge pump remains operational
- XEN is a logic output representing the state of the driver:
  - XEN = HI when OUT is LO (SiC MOSFET is OFF)
  - Fault detection; (PWM & XEN)=HI

VEESET=SGND → OFF
VEESET=OPEN → -3.5V
VEESET=V5V → -5V
VEESET=SVDD → -8V

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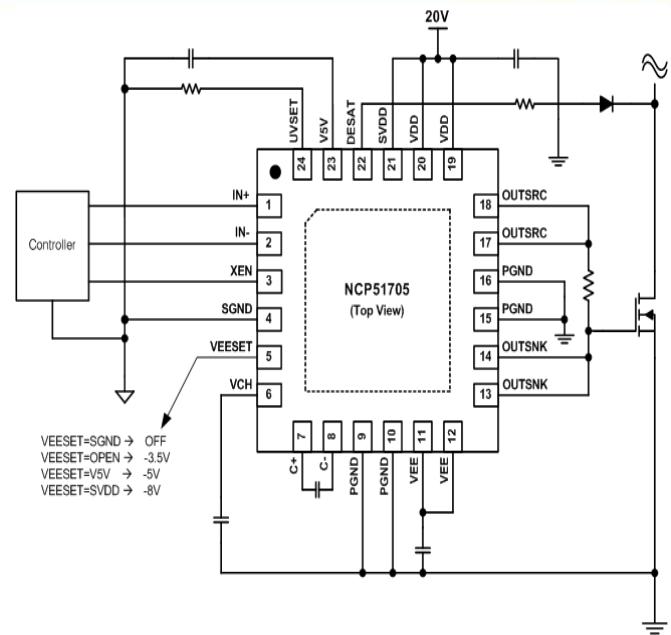ON Semiconductor®

NCP51705 Driver Implementation – OUT pins

- NCP51705 a split output stage:
  - independent turn-on and turn-off speed adjustment by external R
  - Low source/sink impedance; R_{OUT} = ~5Ω (max.)
  - 1 pull-up device
  - 2 pull down devices fired 40ns part
- High peak current capability (+/- 6A)
- High frequency operation up to 500 kHz
  - High Q_G combined with high frequency might yield a thermally limited design → disable charge pump to extend frequency range
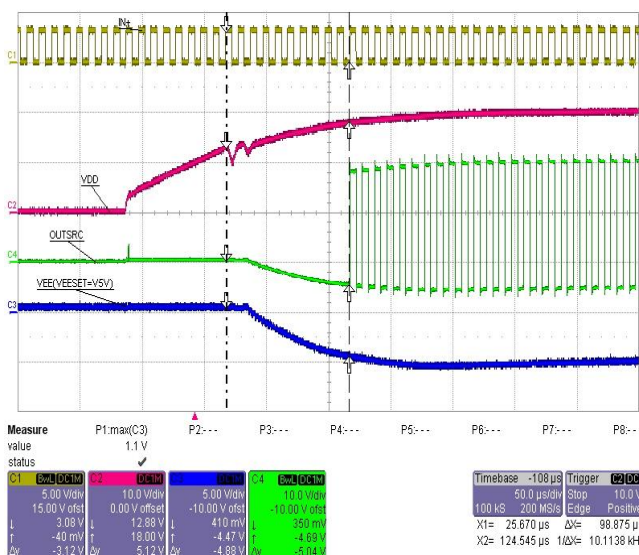

VEESET=SGND → OFF
VEESET=OPEN → -3.5V
VEESET=V5V → -5V
VEESET=SVDD → -8V

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NCP51705 Driver Implementation – DESAT

NCP51705 DESAT functionality:

➢ DESAT sense is blanked during the off-time and the first 500ns of the on-time

➢ During blanking the DESAT pin is pulled to GND by an internal switch.

➢ DESAT to OUT delay is estimated to be ~50ns

➢ DESAT protection is not an accurate protection due to blocking diode and R_{DSON} characteristics

➢ Threshold is 7.5V at the pin; V_{DS} trip point can be adjusted by the voltage drop across R – D combination.


VEESET=SGND → OFF
VEESET=OPEN → -3.5V
VEESET=V5V → -5V
VEESET=SVDD → -8V

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Operating Waveforms (1/6) - Startup

Notable:

➢ UVLO is edge triggered; first pulse is guaranteed to be a full pulse

➢ Negative bias is generated from VDD and monitored for sufficient level before operation is enabled
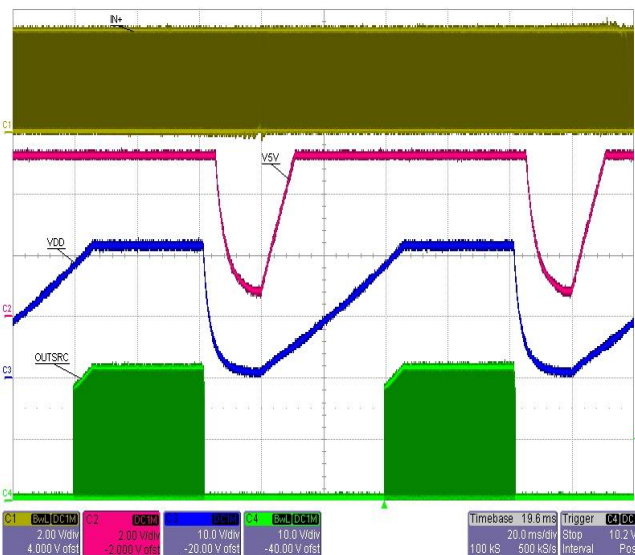
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Operating Waveforms (2/6) – Shut down
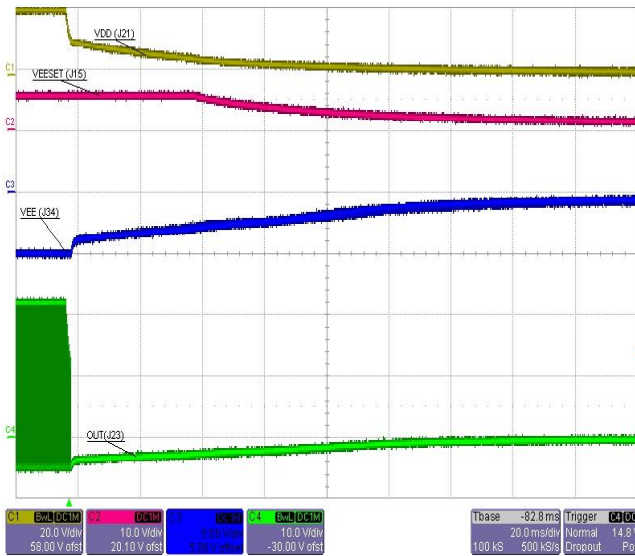
Notable:

➢ **Clean last pulse**

➢ **No glitches after UVLO is activated**
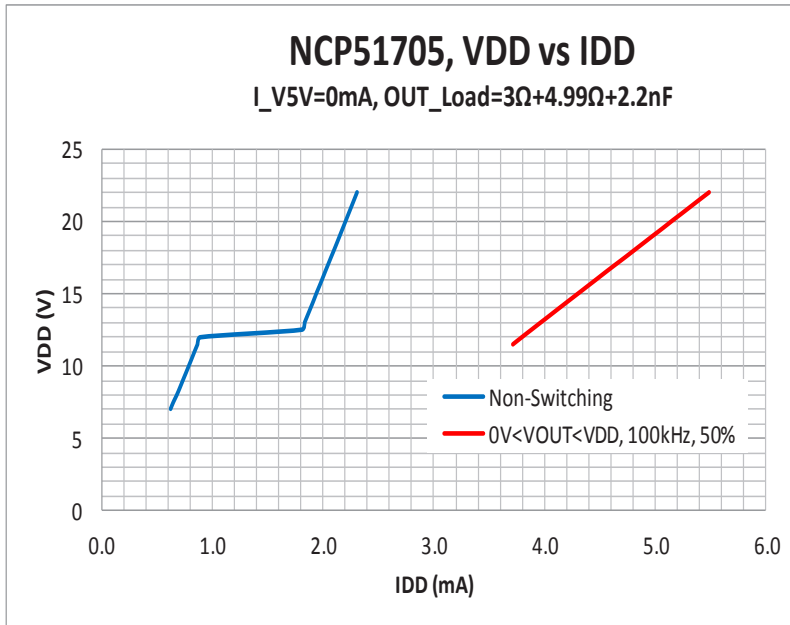
➢ **Internal hysteresis is ~1V (fixed)**

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Operating Waveforms (3/6) – Power Cycling

Notable:

➢ **Clean ON – OFF cycles**

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Operating Waveforms (4/6) – Power Consumption

NCP51705, VDD vs IDD
I_V5V=0mA, OUT_Load=3Ω+4.99Ω+2.2nF

Legend:
- Non-Switching
- 0V<VOUT<VDD, 100kHz, 50%

X-axis: IDD (mA)
Y-axis: VDD (V)

Notable:

➢ **Charge pump is disabled in this measurement.**

➢ **(4.99Ω + 2.2nF)** is the equivalent circuit of a typical SiC transistor

➢ **3Ω** is the external gate resistor used
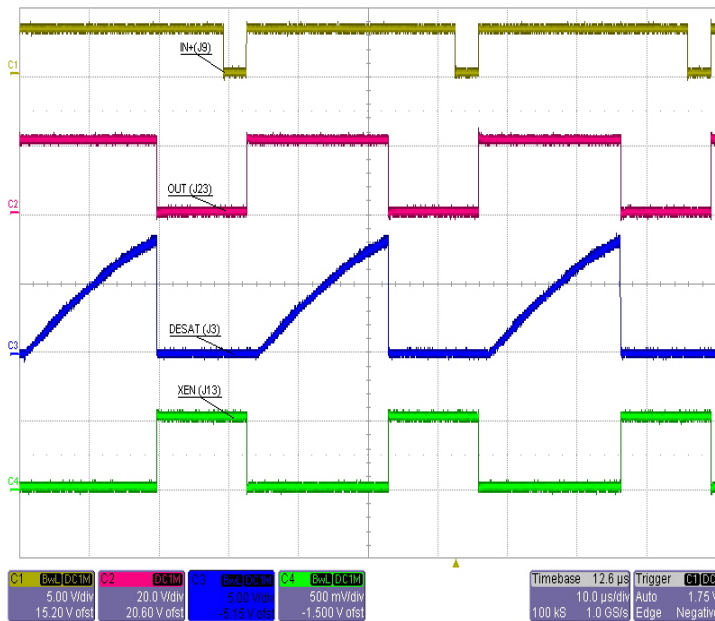
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Operating Waveforms (5/6) – Dynamic Behavior
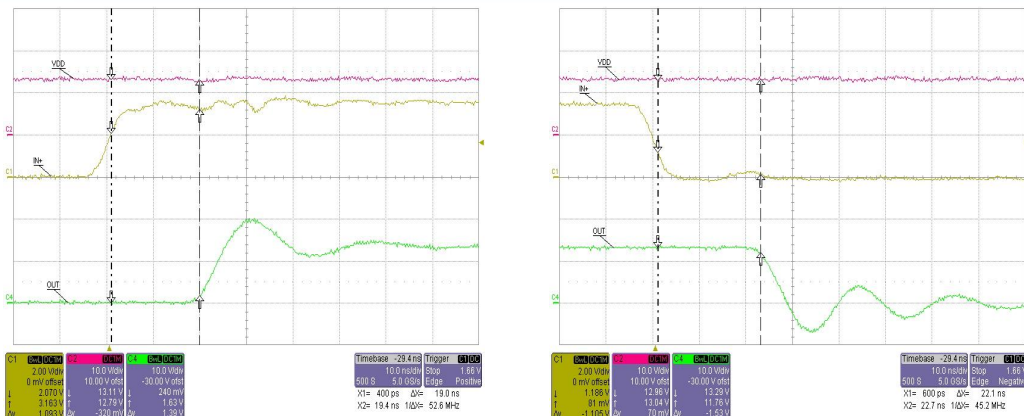
Notable:

➢ **Turn-On propagation delay: ~19ns; Output rise time: ~5ns (load is 1nF)**

➢ **Turn-Off propagation delay: ~21ns; Output fall time: ~5ns (load is 1nF)**

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Operating Waveforms (6/6) – DESAT Protection

Notable:

➢ **Output is terminated before the PWM input goes low when DESAT pin voltage reaches the threshold**

  • **~7.5V in DESAT mode**

  • **~1.25V in CS mode**

➢ **Used a very shallow ramp – no chatter is observed.**

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Applications – GND referenced, single ended
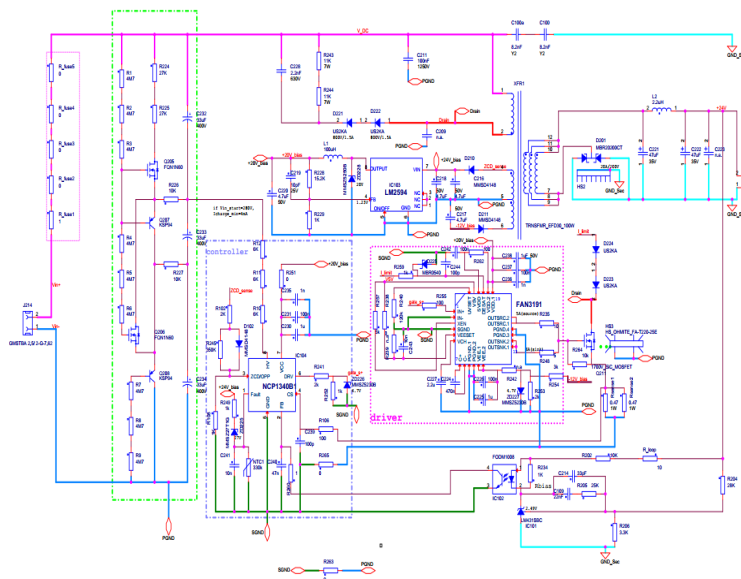

➢ **Up to 900V input, 100W, 24V output auxiliary power supply**

➢ **QR flyback**

➢ **Up to 400kHz switching frequency**

➢ **Fully operational with external power supply for control circuit**

➢ **Working on board further optimization**

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# Applications – Isolated Half-Bride Concept

- ➢ High power applications prefer isolated drivers for both, the high side and the low side.

- ➢ Must use 2 digital isolator devices .

- ➢ Cross conduction prevention, dead time adjustment, fault management must be implemented in the digital domain.

- ➢ In most cases temperature sensing and thermal management are also done by the digital controller.
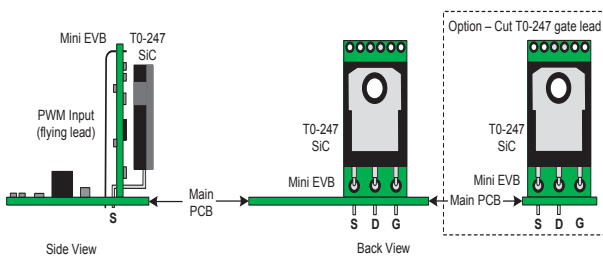
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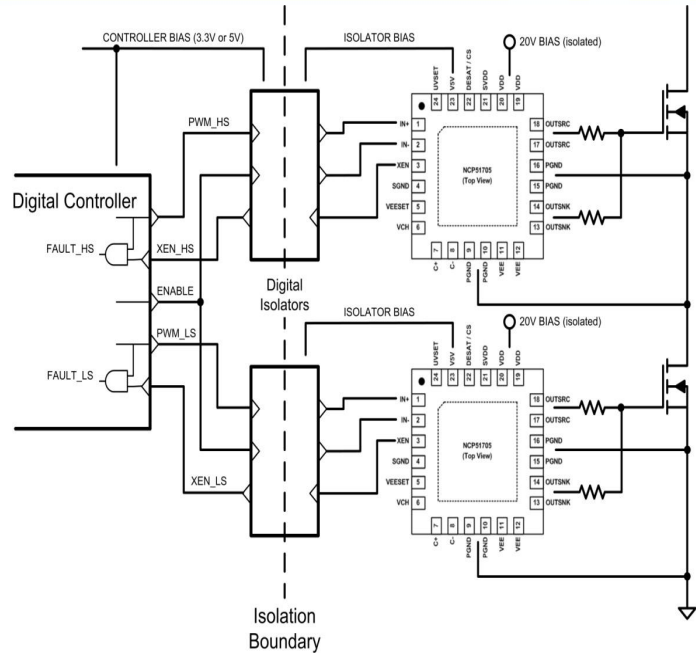
Customer Evaluation Board

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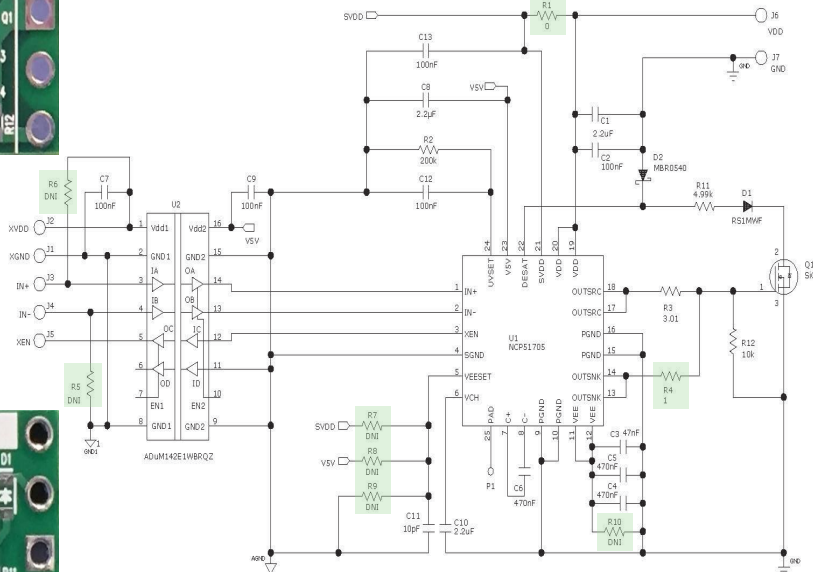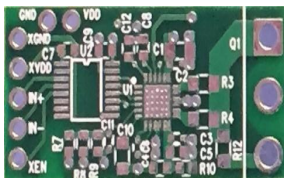
NCP51705 Mini EVB Mounting
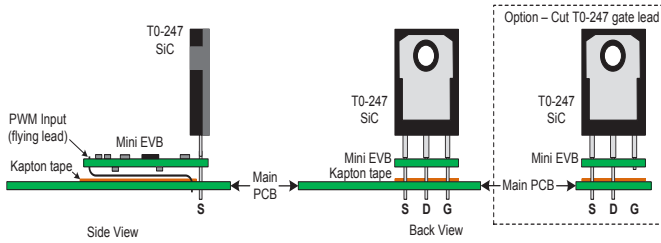
Option 1 (preferred) – Horizontal mounting

Option 2 – Vertical mounting

- Mounting into existing power PCB
- Hardwire to EVB
  - XVDD/XGND (digital isolator primary + 5 V)
  - V_{DD}/GND (NCP51705 + 20 V)
  - IN+ /XGND (PWM input signal)

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