순환전류와 다이오드 역회복 전류가 작은 인터리빙 방식의 새로운 ZVS 토템폴 PFC 컨버터

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A novel ZVS interleaved totem-pole PFC converter with reduced circulating current and diode reverse recovery current

ABSTRACT

This paper introduces a novel ZVS interleaved totem-pole PFC with the reduced circulating current and the reverse recovery current of the diodes. With the help of a simple auxiliary inductor, both ZVS turn-on of the main switches and soft turn-off of the body diodes can be achieved. In the proposed totem-pole PFC topology since the switching losses and the reverse recovery losses can be significantly reduced, the typical Si MOSFETs can be employed. In addition the circulating current is reduced by adjusting the switching frequency. The proposed PFC topology can be a low cost solution to achieve high efficiency in high power PFC applications. The validity and the feasibility of the proposed topology is verified by the experimental results with a 3.3kW interleaved totem-pole PFC converter.

Index Terms – digital control, high power PFC, interleaved totem-pole PFC, reverse recovery, ZVS turn-on

1. Introduction

High efficiency is the most important concern in any power conversion systems. Many of the typical power conversion systems connected to the AC grid such as electric vehicle chargers and the DC power supplies for the data center are composed of a front-end PFC converter and a following DC-DC converter. The state-of-the-art DC-DC converters have developed with several matured soft switching techniques such as a phase shift switching technique and a resonant switching technique, and thus the DC-DC converter can exhibit a high efficiency in a compact size. However, in case of the PFC it is difficult to achieve the soft switching over the wide range of operating point without the help of complex auxiliary circuit. This makes it difficult to adopt soft switching techniques for the PFC converters and hence the most of the high power PFC converters employs hard switching techniques[1]. Therefore, the switching frequency of PFC is typically limited below 100kHz as it is a trade-off between the size and the efficiency. Consequently, the size of the whole system is decided by the size of the PFC stage.

Recently, the totem pole PFC has got much attention due to its simple structure and bidirectional power flow capability. In addition the lower number of the component counts on the power path contribuites to a reduction in the conduction losses. However, this topology can hardly be implemented with typical Si MOSFETs due to the severe reverse recovery problem of the body diodes. Typically, the totem pole PFC is developed with IGBTs or wide bandgap devices such as SiC MOSFETs and GaN MOSFETs due to its small reverse recovery current [2]. With the help of a significant reduction in the conduction losses, a totem pole PFC converter implemented with GaN MOSFETs can achieve very high efficiency with high input voltage. However, since the switching frequency and the volume of the converter is in a trade-off relationship due to the hard switching scheme, it is difficult to reduce the volume of the converter below a certain limit. In the Ref. [3] the low cost Si MOSFETs are employed in the totem pole PFC by reducing the reverse recovery current of the body diode in the MOSFET switches. Though the additional fast diodes are used to reduce the losses due to the reverse recovery current, a large forward voltage drop of the external diode contributs to a large conduction loss of the converter.

In order to reduce the switching losses at high power applications, the soft switching technique is essential. The most popular method to achieve ZVS in a totem pole PFC is to operate it in the discontinuous conduction mode [4]. However, the accurate synchronization between the phases is required for the interleaved topology and it is being investigated as to how to reduce the severe EMI problem of the converter.

In this paper, a novel interleaved totem-pole PFC with full range of ZVS region is proposed as shown in Fig.1. The proposed topology employs an additional auxiliary inductor which makes it possible to achieve both ZVS turn-on of the main switches and soft turn-off of the body diodes of the synchronous rectifier MOSFETs. Thus the low cost Si MOSEFT can be used. In addition the circulating current can be reduced by adjusting the switching frequency. Since the frequency control works as an independent loop with controlled variables, it does not cause a stability issue of the control.

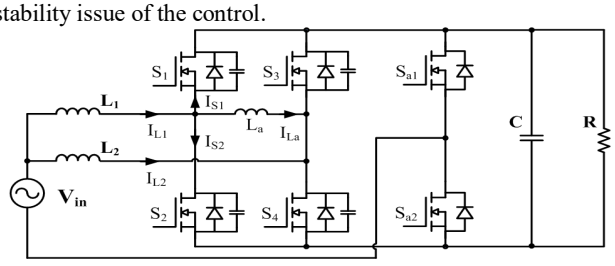


Fig. 1 Proposed ZVS interleaved totem-pole PFC topology

2. Operation of proposed PFC

Since the switching frequency is much higher than line frequency, the operation of the proposed PFC converter can be described in a half of line cycle with duty > 0.5 and duty < 0.5. In the analysis of the circuit operation it is assumed that the switches are ideal except the the body diode and the parasitic output capacitcance to investigate the ZVS turn-on of main MOSFET switches and the reverse recovery of the body diodes. The circuit operation is analyzed in the positive half of line cycle, where S_2 and S_4 are the main boost switches, S_1 and S_3 are the synchronous rectifiers and S_{a2} is a line connected switch. The key waveforms are shown in Fig. 2 when the duty is greater than 0.5. It can be observed from the Fig. 2 that the main switch S_2 can achieve ZVS turn-on and the body diode of synchronous rectifier S_1 can achieve the soft switching turn-off during the positive half of line cycle. The circuit operation with duty < 0.5 is omitted here since it is similar to that with duty > 0.5. In the negative half of a line cycle, S_1 and S_3 are the main boost switches, S_2 and S_4 are synchronous rectifiers and S_{a1} is a line connected switch. Due to the symmetric operation characteristics, the operation in the negative half of a line cycle is omitted.

3. Soft switching condition and circulating current reduction technique with frequency control

A. ZVS condition design

From the above operation, the ZVS condition is guaranteed if the inductive energy of the auxiliary inductor E_{La} is sufficient

enough to provide its current to cancel the current of the input inductor connected to the leg involved in the commutation and discharge the capacitive energy E_{oss} in the output capacitors of MOSFETs in the same leg as shown in Eq. (1).

$$\frac{1}{2}L_a\left(I_{La}-I_{Lin}\right)^2 \geq 2\left(\frac{1}{2}C_{OSS}V_o^2\right) \quad (1)$$

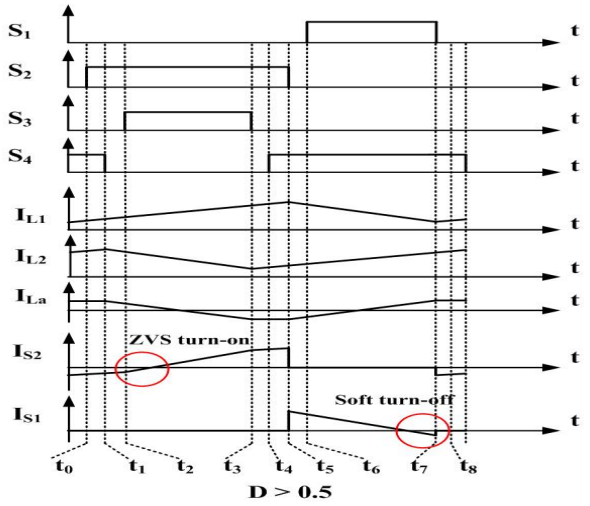


Fig. 2 Key waveforms when duty is greater than 0.5 in the half positive of line cycle.

From Eq. (1), the worst case scenario occurs when the inductor current is the maximum. Assuming that the unity power factor is achieved and the input current is shared equally in two interleaved phases of the PFC converter, the input inductor current reaches the maximum value at the peak of input voltage and it is equal to a half of peak input current. At the end of power transfer interval in interval 7 (t_6~t_7) the equation for the ZVS can be derived by Eq. (2). Here, the dead time period is neglected in the ZVS design for simplification.

The minimum value of required auxiliary inductance can be obtained by Eq. (2) under the assumption that $L_1 = L_2 = L_{in}$.

$$\frac{1}{2}L_a\left[\frac{1}{2}\frac{V_{inL\_pk}}{L_a f_s}-\left(\frac{P_{in}}{V_{inL\_pk}}-\frac{V_{inL\_pk}\left(1-\frac{V_{inL\_pk}}{V_O}\right)}{2L_{in}f_s}\right)\right]^2 \geq C_{OSS}V_O^2 \quad (2)$$

Where, V_{inL_pk} is the peak input voltage.

B. Circulating current characteristic

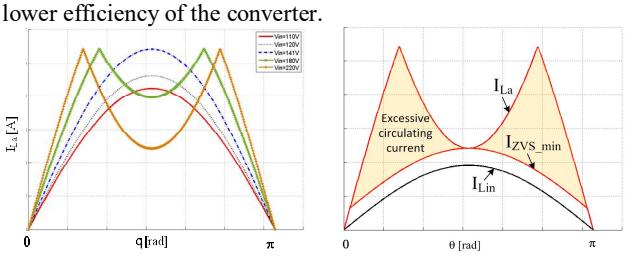
During a half of a line cycle, the input sinusoidal voltage varies from zero to its peak value. Thus the duty is also changed from zero to the peak value. The peak value of the circulating current can be calculated by Eq. (3).

$$I_{La\_pk}=\begin{cases}\frac{1}{2}\frac{V_o}{L_a}DT_s & when\ D>0.5\\ \frac{1}{2}\frac{V_o}{L_a}(1-D)T_s & when\ D<0.5\end{cases} \quad (3)$$

The variation of circulating current in a half of a line cycle is shown in Fig.3 with the input voltage variation from 110V to 220V when the output voltage is 400V.

From (1), the minimum value of required circulating current for ZVS condition can be derived as Eq. (4). Since the PFC operates in CCM mode and the ripple current I_{Lin} is small as compared to the input current, the required circulating current for the ZVS operation in Eq. (4) is proportional to the input current.

It can be noticed from Fig.3 (a) that the circulating current is proportional to the input current when the input voltage is smaller than 141V, thus there is no problem in achieving the ZVS operation. However, when the input voltage is higher than 141V, the relationship becomes nonlinear. In order to achieve the full range ZVS operation of the proposed totem-pole PFC, the circuit has to be designed in such a way that the lowest value of the circulating current exceeds the peak value of the input current. However, if a fixed switching frequency is used for the converter, then the circulating current is excessive during the most of the time in a half of a line cycle as shown in Fig. 3 (b), resulting in a lower efficiency of the converter.



(a) (b)

Fig. 3 Variation of circulating current in a half of a line cycle; (a) circulating current variation with input voltage variation (b) excessive circulating current when input voltage > 141 V.

$$I_{La\_ZVS}=I_{Lin}-0.5\times\Delta I_{Lin}+\frac{C_{OSS}V_O}{t_d} \quad (4)$$

$$\text{Where}\quad \Delta I_{Lin}=\frac{V_{in}}{f_s L_{in}}\left(1-\frac{V_{in}}{V_O}\right) \quad (5)$$

C. Circulating current reduction technique with frequency control

In order to reduce the circulating current, the switching frequency can be adjusted. In the design process, the circulating current can be optimized according to the input current reference (i.e. power of PFC) to satisfy the ZVS condition in Eq. (5). The optimal frequency to reduce the circuilating current can be calculated by Eq. (6).

$$f_{sb}=\frac{V_{in}L_{in}+V_{in}\left(1-\left(V_{in}/V_O\right)\right)L_a}{I_{Lin\_ref}+2C_{oss}V_O/t_d} \quad (6)$$

Then the switching frequency needs to be adjusted in a half of a line cycle. As long as the instantaneous value of the input voltage is lower than a half of the output voltage (i.e. duty is greater than 0.5), the switching frequency is maintained at a constant value f_{sb}. When the input voltage is greater than a half of the output voltage, the switching frequency f_s is adjusted by the Eq. (7) in order to shape the circulating current to follow the envelope of the input inductor current.

$$f_s=\frac{1-\left(V_{in}/V_O\right)}{V_{in}/V_O}f_{sb} \quad (7)$$

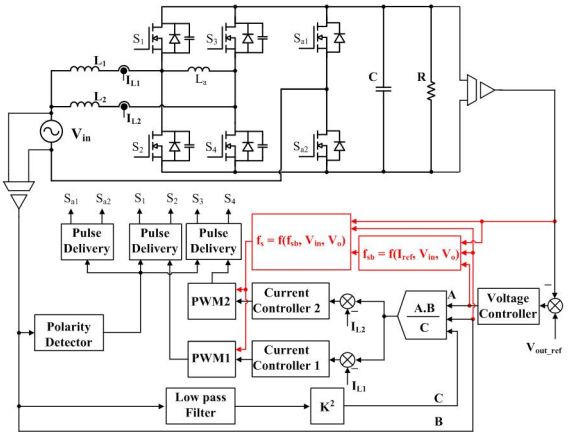


Fig. 4. Control scheme for the proposed PFC

Fig. 4 shows the control scheme for the proposed PFC converter based on the average current control method. The control scheme consists of two cascaded loops. The outer voltage loop regulates the output voltage and provides the current reference signal to the current controller. Two identical current controller regulate the inductor current in each phase of PFC converter.

4. Experiment results

In order to verify the operation of the proposed PFC, a 3.3 kW PFC converter is implemented. The specification of the proposed PFC converter is shown in Table 1.

Table 1 Specification of the proposed 3.3 kW PFC converter

Parameter	Symbol	Value
Rated power	P	3.3 kW
Input voltage	V_{ac}	110, 220V
Switching frequency	f_{sw}	(70~200)kHz
Input inductor	L_{in}	200 μH
Auxiliary inductor	L_{aux}	50 μH

Fig. 5 and Fig.6 show the key waveforms of the proposed PFC converter with two different V_{in}, 220V and 110V, respectively. In both cases the input current tracks the input voltage well and exhibits a high input power factor. The switching frequency is varied in between 70kHz and 200kHz in a half of a line cycle at 220V.

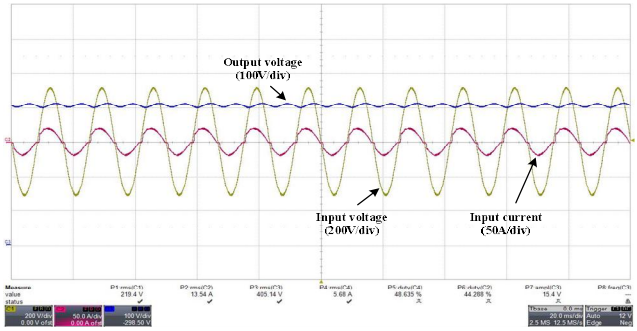


Fig. 5. Key waveforms of the proposed PFC converter at 3.3kW with 220V input voltage.

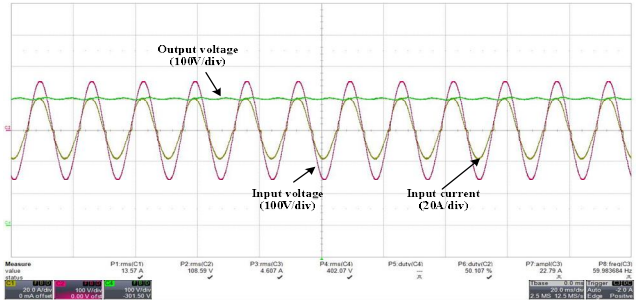


Fig. 6. Key waveforms of the proposed PFC converter at 1.5kW with 110V input voltage.

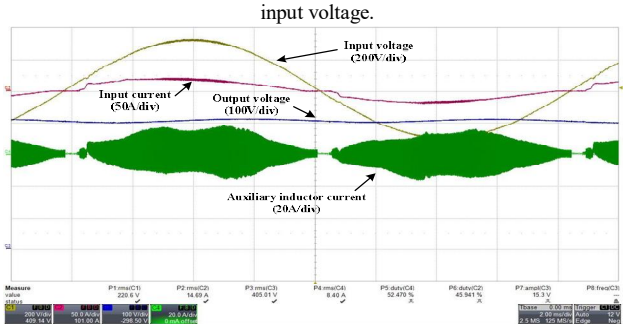


Fig. 7. Auxiliary inductor current waveforms of the proposed PFC converter at 3.3kW with 220V input voltage.

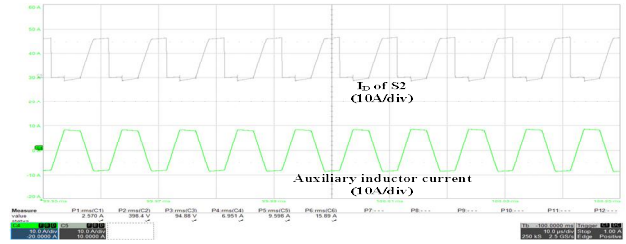


Fig. 8. Switching waveform of auxiliary inductor current and active boost MOSFET S2 in the proposed PFC converter at 3.3kW with 220V input voltage.

Fig.7 shows the waveform of auxiliary inductor current in the proposed PFC converter with 220V input voltage at full load. By using the proposed frequency adjustment technique, the auxiliary current is reduced to 8.4A at full load with 220V input voltage. The detail switching waveforms of the auxiliary inductor current and the main active boost switch are shown in Fig. 8. It can be observed that the main MOSFET S_2 achieves the ZVS turn-on.

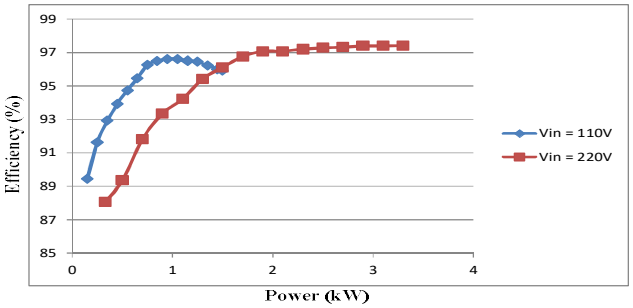


Fig. 9 Key waveforms with V_{in} = 220V at P_{out} = 6.6 kW

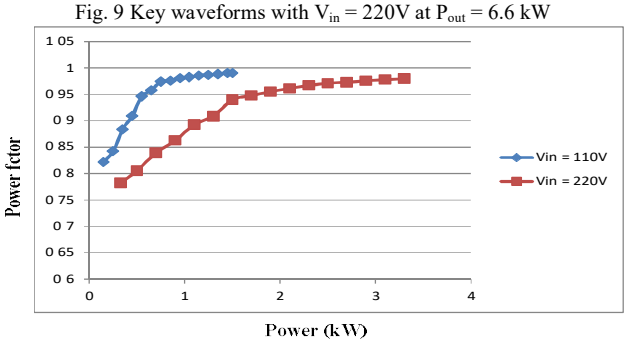


Fig. 10 Key waveforms with V_{in} = 220V at P_{out} = 6.6 kW

The efficiency and power factor profiles of proposed PFC are shown in Fig.9 and Fig.10, respectively. The proposed PFC shows high efficiency with high switching frequency operation at both low and high line input voltage. The peak efficiency of the proposed topology is 97.4% with 220V input voltage at full load. The power factor reaches 0.99 at low line voltage.

5. Conclusion

In this paper a novel ZVS interleaved totem pole PFC converter with reduced circulating current and diode reverse recovery current has been proposed. The superior characteristics of the proposed converter can be summarized as follows: an inherent lower conduction losses due to the small number of devices on the power path, significant reduction of reverse recovery current of the body diode in the synchronous rectifier, full range ZVS turn-on of main switches, the reduced circulating current by the frequency control technique. It can be concluded that the proposed topology is highly suitable for high power PFC applications. All the superior features of the proposed topology has been verified with a 3.3kW prototype circuit.

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