Modeling and Control of ISOP Active-Clamp-Forward Converter for xEV Low Voltage DC/DC Converter

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ABSTRACT

This paper present an input series output parallel active clamp forward converter for low voltage dc/dc xEV application. The converter can achieve ZVS turn on for all switches. An accurate small signal model of the converter which includes the effect of leakage inductance is given and controller design based on modeling is described. Experimental and simulation results from a 3.2kW, 100kHz prototype are presented in order to verify the validity of the converter operation and the designed control parameters.

1. Introduction

In xEV, to power the 14V auxiliary loads, such as radio, power window, and to charge low voltage battery, an isolated low voltage dc/dc converter (LDC) is used. The LDC, with power range of a few kilowatts (1kW ~ 5kW), converted the power from high voltage bus (260V ~ 440V) to the 14V low voltage bus. The system configuration of a typical xEV is shown in Fig.1.

Phase shift full bridge (PSFB) converter is considered as the most popular topology for this application [1]. However, high turn ratio is needed to achieve the high step down ratio of LDC application. Therefore, it will increase the duty loss as well as circulating current.

Input series output parallel (ISOP) configuration can be applied to decrease the transformer turns ratio. However, applying ISOP configuration to PSFB converter leads to high number of switches.

In this paper, an ISOP active clamp forward converter (ACFC) is selected for this application, because it can achieve similar performance with PSFB converter with reduced number of switches. A good control design is needed to achieve high reliability, which is typically a requirement for automotive application. Thus, a controller design based on a more accurate small signal model is provided.
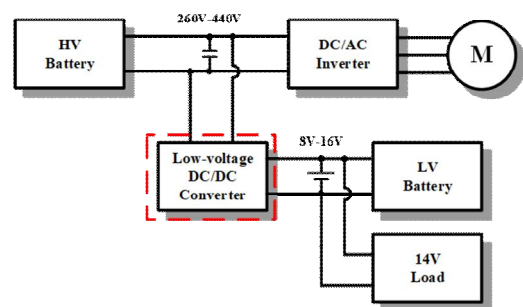

Fig.1 Typical xEV system.

2. Modeling and Control Design of ISOP ACFC

2.1 Modeling of ISOP ACFC

Fig.2 shows the circuit diagram of ISOP ACFC. It can be seen that the structure of the converter is consists of two ACFC which are connected in ISOP configuration.
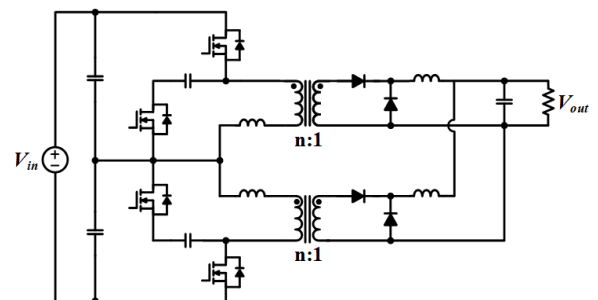

Fig.2 ISOP ACFC.

In ISOP ACFC, the working principle of upper and lower converter are the same with 180° phase shift operation. Thus, small signal model of a single ACFC with half of rated power is sufficient to design the controller.

Fig.3 shows the key waveform of ACFC which consists of four modes of operation. In most of literatures, ACFC is modeled by neglecting the effect of leakage inductance that leads to only mode 2 and mode 4, which the model will be the same with conventional buck converter model [2] [3]. This assumption will decrease the controller design accuracy.

This paper adopt the modeling technique used in [4], which will retain the information of leakage inductance. The

procedure is to first derived the fast variable equation of leakage inductance current. From mode 1 and 4, a is derived and from mode 2 and 3, β is derived. a and β retain the leakage inductance information and will be embedded into averaged slow variables state equations which consist of output inductor current, output voltage, magnetizing current, and clamp capacitor voltage.

Next step is to linearize the slow variables state equations using small signal technique. The inductor current to duty cycle is derived as in eq(1) and the inductor current to output voltage formula is shown in eq(2). Eq(1) and (2) represents a more accurate model of ACFC which includes the effect of leakage inductance.
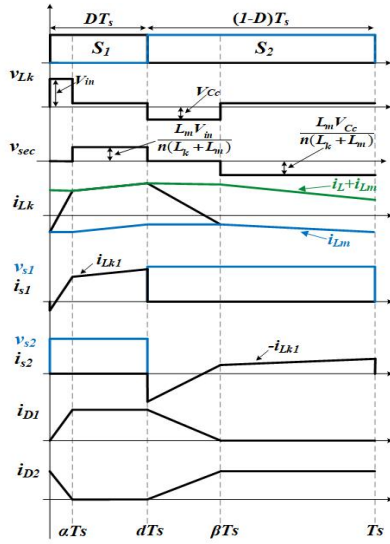
$$G_{vi}(s) = \frac{R}{1 + sRC} \tag{2}$$

Fig.3 Key waveform of ACFC

2.2 Controller design

Inner current loop outer voltage loop control structure is used to control ISOP ACFC. Fig.4 shows the control structure with the power stage transfer functions. The dynamic specifications is given in Table 1.

Table 1 Dynamic specifications

Item	Specification	Remarks
Gain margin	>6dB	
Phase margin	>50°	
Load regulation	±10% overshoot and undershoot	With 2ms 10% to 90% load ramp change
Line regulation	±10% overshoot and undershoot	With 5ms 260V to 440V ramp change

Both outer and inner loop control are designed using classical PI controller. Table 2 summarize the components value, which are used in the model. The maximum allowable bandwidth from the MCU is 8kHz. For inner loop controller the value of Kp = 0.0068 and Ki = 549, which result in bandwidth of 7.1kHz. As for outer loop controller the value Kp = 0.58 and Ki = 83694, which result in bandwidth of 1.7kHz. Using MATLAB, the frequency response of inner and outer loop is given in Fig.5 and Fig.6. It can be seen that the phase and gain margin requirement are fulfilled using the design value of PI controller.

Table 2 Passive components value

Item	Value	Item	Value
L	10uH	Cc	1uF
C	47uF	Lk	7uH
Lm	100uH	n	4

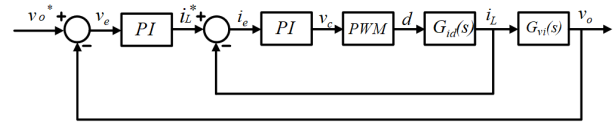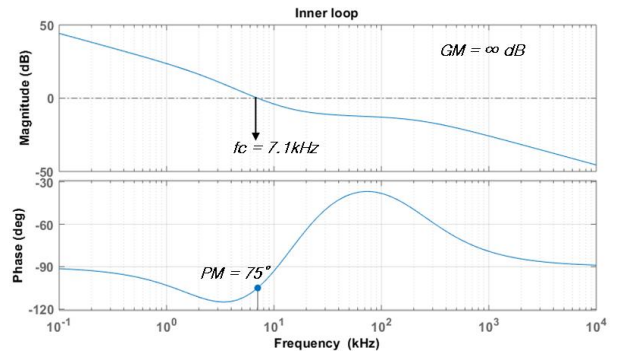Fig.4 Double-loop control system
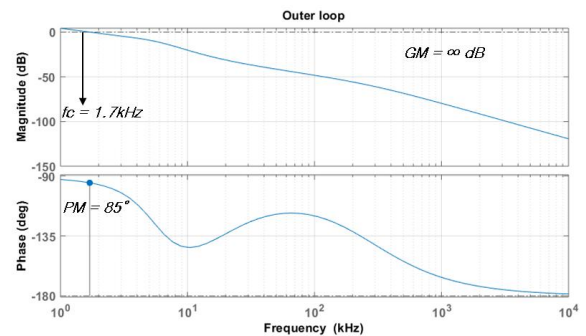

Fig.5 Frequency response of inner loop

Fig.6 Frequency response of outer loop

$$G_{id}(s) = \frac{nVinL_m(1 + sRC)}{s^2[n^2LCR(L_m + L_k)] + s[RCL_mL_kf_s + n^2L(L_m + L_k)] + [L_mL_kf_s + n^2R(L_m + L_k)]} \tag{1}$$

3. Simulation and Experimental Results

The prototype of 3.2kW, 100kHz of ISOP ACFC is used to verify the converter operation and it is shown in Fig.6. Planar transformer is implemented in the prototype in order to achieve low profile converter system. Extra leakage inductance is added to each ACFC in order to achieve soft switching in all operating condition. The steady state experiment results is shown in Fig.7. From Fig.7 (a) it can be seen that the two ACFC connected in ISOP configuration is well balanced both in output current and input voltage, and it shows the 180° phase shift operation. From Fig.7 (b) the soft switching performance can be observed from the leakage inductor current, which represent the switch current. The leakage inductor current is negative when the switch voltage is zero, thus ZVS turn on is achieved. The simulation results for the dynamic response using the design controller value in the previous section are shown in Fig.8. It can be seen that the overshoot/undershoot voltage under ramp load change is only 1V and negligible overshoot/undershoot under line ramp change. Thus, it can be concluded that the controller design is able to meet the required dynamic specifications.
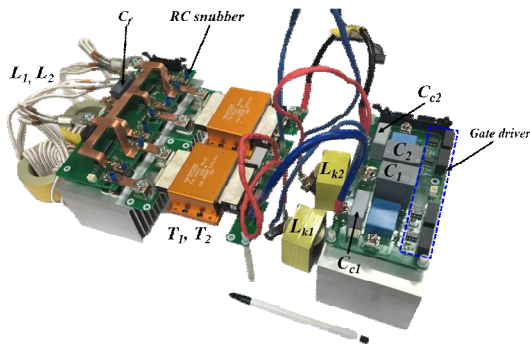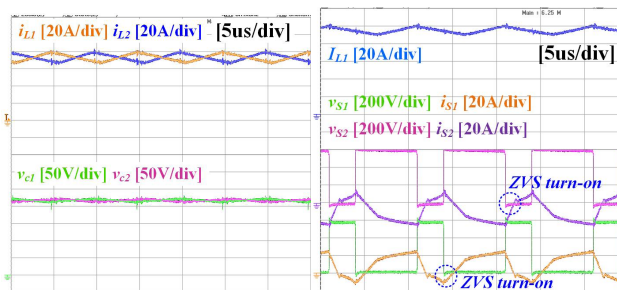

Fig.6 Prototype of the proposed ISOP ACFC

(a) Interleaving waveform   (b) Soft-switching performance
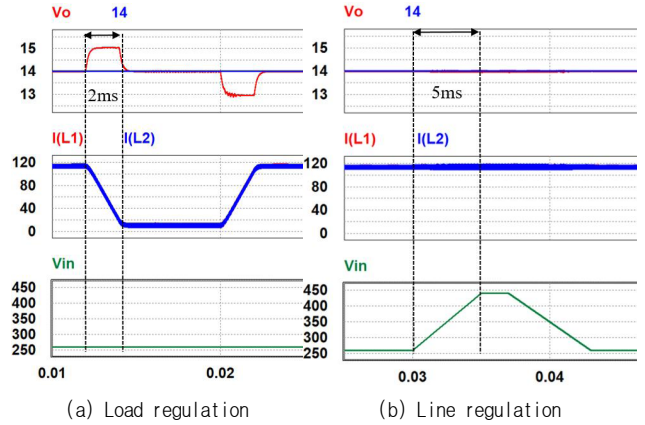
Fig.7 Steady-state operation

(a) Load regulation   (b) Line regulation

Fig.8 Simulation of dynamic responses

4. Conclusion

In this paper, an ISOP ACFC is implemented for xEV 400V/14V LDC. The proposed converter for LDC have more advantages compared to the coventional PSFB converter. ZVS turn on is achieved for all switches and ZCS turn off is achieved for all diodes. A more accurate modeling which includes the effect of leakage inductance is derived. Moreover, model based controller design is provided. Experimental and simulation results of ISOP ACFC are given from 3.2kW, 100kHz prototype to validate the operation of the converter.

References

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