# 디지털 록인앰프를 이용한 비정현 계통하에서 강인한 PLL 방법

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# A Robust PLL Technique Based on the Digital Lock-in Amplifier under the Non-Sinusoidal Grid Conditions

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## ABSTRACT

The harmonics and the DC offset in the grid can cause serious synchronization problems for grid connected inverters (GCIs) which leads not able to satisfy the IEEE 519 and p1547 standards in terms of phase and frequency variations. In order to guarantee the smooth and reliable synchronization of GCIs with the grid, Phase Locked Loop (PLL) is the crucial element. Typically, the performance of the PLL is assessed to limit the grid disturbances e.g. grid harmonics, DC Offset and voltage sag etc. To ensure the quality of GCI, the PLL should be precise in estimating the grid amplitude, frequency and phase. Therefore, in this paper a novel Robust PLL technique called Digital Lock-in Amplifier (DLA) PLL is proposed. The proposed PLL estimate the frequency variations and phase errors accurately even in the highly distorted grid voltage conditions like grid voltage harmonics, DC offsets and grid voltage sag. To verify the performance of proposed method, it is compared with other six conventional used PLLs (CCF PLL, SOGI PLL, SOGI LPF PLL, APF PLL, dqDSC PLL, MAF PLL). The comparison is done by simulations on MATLAB Simulink. Finally, the experimental results are verified with Single Phase GCI Prototype.

*Index Terms* – Phase Locked Loop, Digital Lock-In Amplifier, Grid Connected Inverter, DC Offset.

## 1. INTRODUCTION

Renewable energy sources are replacing conventional power generation sources due to their clean characteristics and cheap operational costs. Many kinds of environment friendly advantages including zero carbon foot print can be rejoiced if present day grid gets most of its power from the renewable energy resources such as the Photovoltaics, Wind Turbines, Fuel cells and etc. In order to inject the power from the renewable energy sources to the grid, the Grid Connected Inverters (GCIs) need to synchronize their outputs with the grid properly. The synchronization is performed by the Phase Locked Loop (PLL) which is a key component in GCIs control and it has a great influence on the power quality, the stability and the reliability of the power systems. The PLLs are used to estimate the frequency and the phase of the grid voltages in order to synchronize the GCIs with the grid. Therefore, it is essential for the PLL to effectively reject the disturbances such as the harmonics, frequency variations, DC Offsets and phase shifts in the grid voltage even under the power quality events.

Nowadays due to the ever-increasing use of non-linear loads the power quality of the grid gets worse and hence it is more difficult to achieve a perfect synchronization between the GCIs and the grid. Conventional PLLs show good performances in estimating the frequency and the phase of the grid voltage under the sinusoidal and symmetrical grid conditions. However, when it is under the non-sinusoidal grid conditions with harmonics, voltage sags or swells and DC Offset, the precise estimation of phase and frequency becomes highly difficult [1]. Moreover, one of the most important hurdles which makes it difficult to achieve the perfect grid synchronization is the DC offset present in the grid quantities [2]. The DC offsets can be present in the sensed grid quantities due to the inaccuracy of the sensors and ADC conversion, and the unbalanced operation of the GCIs. DC offset can cause the inaccurate estimation of grid parameters which affects to the power quality of GCIs. Eventually, it leads to a violation of the grid standard such as IEEE 1547 [3] which strictly limits the frequency variation, phase variation and DC injection by the GCIs less than 1.2Hz, 20 degrees and 0.5% of the rated RMS current, respectively.

Many kinds of different synchronization methods have been proposed so far to deal with the non-sinusoidal grid conditions. However, as reviewed in [4], most of the methods developed so far shows a good enough performance under harmonics and DC offset condition only if the additional calculation, filtering blocks are added, which results in increasing the computational burden and the complexity of implementation.

To overcome the aforementioned problems of the conventional PLLs under the distorted grid conditions, a novel digital Lock-In Amplifier (DLA) based PLL is proposed in this paper. The proposed PLL is able to perform well even in extremely distorted grid conditions with DC offsets due to its robust performance in the phase detection. It is equipped with a robust Phase Sensitive Detector (PSD) to detect the phase accurately even under extremely polluted grid conditions. The validity of the proposed technique is verified by comparing it with the other six conventional techniques by the simulation and experimental results under the distorted grid conditions.

## 2. PROPOSED DIGITAL LOCK-IN AMPLIFIER

The PLL is composed of three distinct parts such as Phase Detector (PD), Loop Filter (LF) i.e. PI controller and Voltage controlled Oscillator (VCO). Among them PD is the core of all PLLs and the performance of PLL depends heavily on the accurate estimation of the phase error by PD as emphasized in [5]. Therefore, the PLLs can be categorized based on their PD. Fig. 1 shows two conventional method and the proposed method. The conventional methods include the Quadrature Signal Generator based PLLs which have orthogonal signal generation and park transformation-based PD and Product PLL (pPLL) which have product-based PD as shown in Fig. 1 (a) and Fig. 1 (c) shows the proposed method which uses Digital Lock-in amplifier-based PD, also termed as Phase Sensitive Detector (PSD). The PSD detects the phase error based on its homodyne/heterodyne phase detection technique. The PSD is very robust in nature so that it

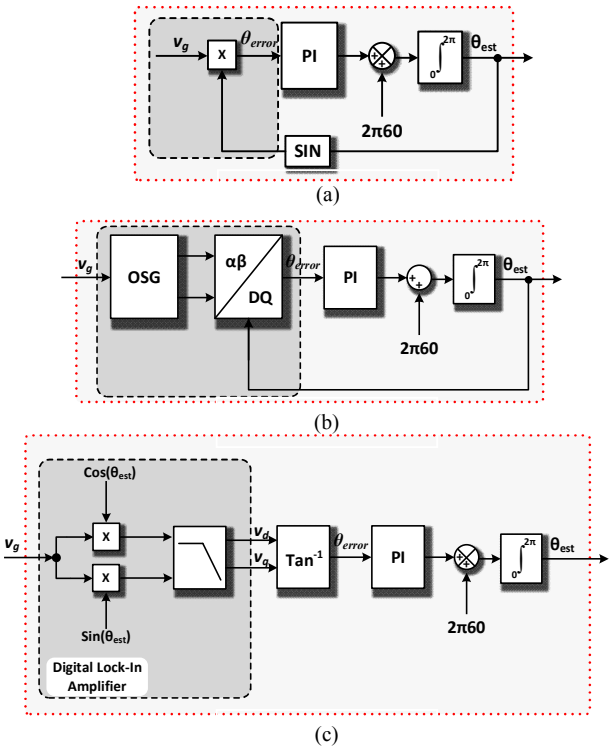


Fig. 1 (a) Conventional OSG based PLL (b) Conventional Product based PLL (c) Proposed Digital Lock-In Amplifier based PLL

can detect the fundamental component of the grid accurately even under very noisy signal conditions. It works on the principle of multiplying the input signal with reference sinusoidal signals to detect the target frequency component. Unlike the other phase detection techniques, PSD extracts only the signal of interest by multiplying the input signal with the reference sinusoidal signal, thereby rejecting all other frequency components. Operation of the PSD will be explained briefly by the equations below.

$$v_g = V_m \sin\left(\omega_g t + \theta_g\right) \quad (1)$$

$$v_{ref} = \sin\left(\omega_{est} t + \theta_{est}\right) \quad (2)$$

$$v'_{ref} = \cos\left(\omega_{est} t + \theta_{est}\right) \quad (3)$$

Where, $v_g$ is the input signal and $v_{ref}$ and $v'_{ref}$ are two 90° phase shifted reference signals for the PSD. Multiplication of the input signal with two reference signals results in two output signals with two different frequencies, a 2nd harmonic ($f_g+f_{ref}$) and a DC ($f_g-f_{ref}$). The DC value contains the phase and the magnitude information of $v_g$.

$$V_x = -\frac{V_m}{2}\begin{pmatrix}\left(\cos\left(\omega_g + \omega_{est}\right)t + \left(\theta_g + \theta_{est}\right)\right) \\ -\left(\cos\left(\omega_g - \omega_{est}\right)t + \left(\theta_g - \theta_{est}\right)\right)\end{pmatrix} \quad (4)$$

(4) is the results of the multiplier which can be obtained by using trigonometric identity. $v_x$ is the output of the multiplier with the reference input as cosine. Whereas, (4) is the intermediate equation where we can approximate the $\omega_g \approx \omega_{est}$ and $\theta_g \approx \theta_{est}$ , after the approximation and simplification we can get the (5), where $\omega_g+\omega_{est}$, $\theta_g+\theta_{est}$, $\omega_g-\omega_{est}$ and $\theta_g-\theta_{est}$ is represented as $\omega_{es}$, $\theta_{est}$, $\Delta\omega$ and $\Delta\theta$ respectively.

(6) and (7) are the final PSD output equations where $v_d$ and $v_q$ are the DQ components i.e. magnitude and phase information of input signal.

As shown in equations it also contains the second harmonic component, in order to get phase and amplitude information from (6) and (7). This second harmonic component is removed by the low pass filter. Hence, the DC component $v_d$ and $v_q$ are extracted which are the outputs of the PSD containing the amplitude and the phase information of the input signal, respectively. $v_d$ and $v_q$ can be used as DQ components which is the another the advantage of DLA PLL that it can inherently generate DQ components without using OSG and Park transformations.

$$V_x = -\frac{V_m}{2}\left(\left(\cos\left(2\left(\omega_{est} t + \theta_{est}\right)\right)\right) - \left(\cos\left(\Delta\omega t + \Delta\theta\right)\right)\right) \quad (5)$$

$$v_d = \frac{V_m}{2}\left(\cos\left(2\left(\omega_{est} t + \theta_{est}\right)\right)\right) + \frac{V_m}{2}\left(\theta_g - \theta_{est}\right) \quad (6)$$

$$v_q = \frac{V_m}{2}\left(\sin\left(2\left(\omega_{est} t + \theta_o\right)\right)\right) \quad (7)$$

Phase error can be calculated using arcTan of $v_d$ and $v_q$, phase error is then fed into loop filter i.e. PI and VCO to generate the appropriate PLL output reference signal for power converters. $v_d$ and $v_q$ contains second harmonics ripple which can be attenuated by use of Low pass filter (LPF), transfer function of LPF is shown in (8).

$$G_{LPF}(s) = \left(\frac{\omega_c}{s + \omega_c}\right)^4 \quad (8)$$

Where $\omega_c$ is the cut off frequency of the Low Pass filter. For the effective removal of remaining harmonics $\omega_c$ should be chosen way lower than the 120Hz at the same time not too less so that overall system would become sluggish. In proposed technique 4th order filter with the cut off frequency is chosen around 35Hz which ensures optimal attenuation, dynamic and steady state performance. After low pass filtering, ArcTan is used to extract phase information from $v_x$ and $v_y$.

PI controller is designed for DLA, an integrator and zero is added at (s+1.033/23.94) in Laplace domain, overall dynamic and steady state response of DLA with the inclusion of PI is adequate with the gain margin 15dB at 5.57Hz phase margin of 72.5 degrees at 10 Hz.

## 3. SIMULATION AND EXPERIMENTAL RESULTS

Proposed technique is simulated on MATLAB Simulink along with the other six conventional PLLs under the non-sinusoidal condition with grid having 3rd, 5th and 7th harmonics same amplitude as of real grid. Real grid harmonics is measured through spectrum analyzer and later added in the simulation. Moreover, simulation results are validated through the hardware experiments using GCI connected to real grid, inverter controller board have Digital Signal Processor (DSP) TMS320F28335 and DAC circuit using MAXIM 541. PLL internal variables like output frequency, output theta and phase error are displayed on the oscilloscope through DAC circuit. Initial delays of SOGI and filters are ignored, therefore measurements are taken after 0.1s to check PLLs performance in steady state. In both hardware and simulation results, from 0.1 to 0.2s grid is non-sinusoidal and 0.2 to 0.3s grid sag event of 0.8pu is introduced and from 0.35 to 0.5 DC offset is added of 0.1pu amplitude. As shown in simulation and hardware results i.e. Fig. 2. and Fig. 3, performance of PLLs suffers greatly under non-sinusoidal condition but it gets more when voltage sag occurs or there is a DC Offset in measurement. On contrary DLA-PLL shows very less frequency and phase variations in all conditions which is 0.2Hz and 0.5 degrees respectively. PI parameters of the Lock-In based PLL are designed to achieve optimal dynamic and steady state performance. It is evident from simulations and experiments, conventional techniques suffer an unacceptable phase and frequency variations error under harmonics, voltage sag and DC offset which is against the IEEE standard however, DLA-PLL

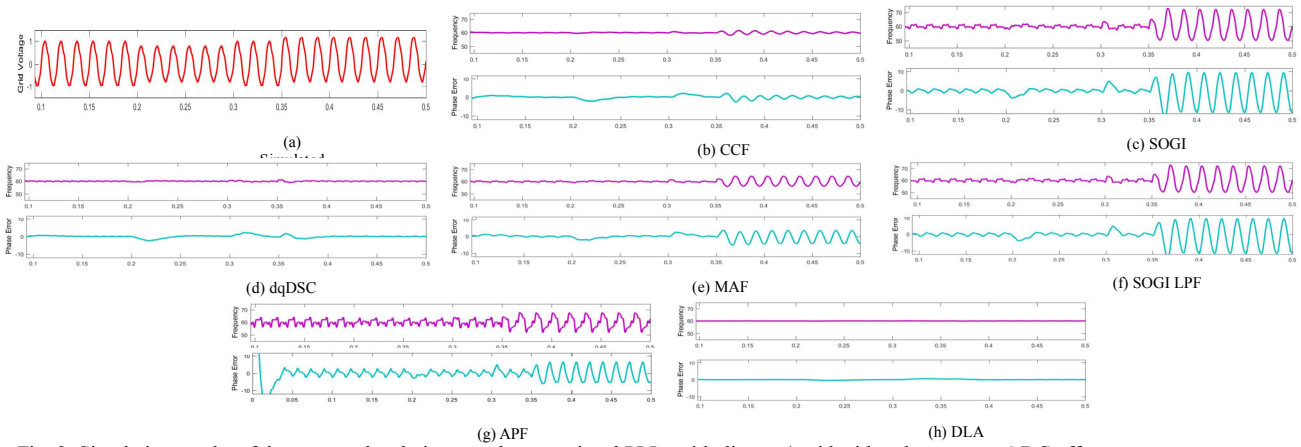


Fig. 2. Simulation results of the proposed techniques and conventional PLLs with distorted grid with voltage sag and DC offset.

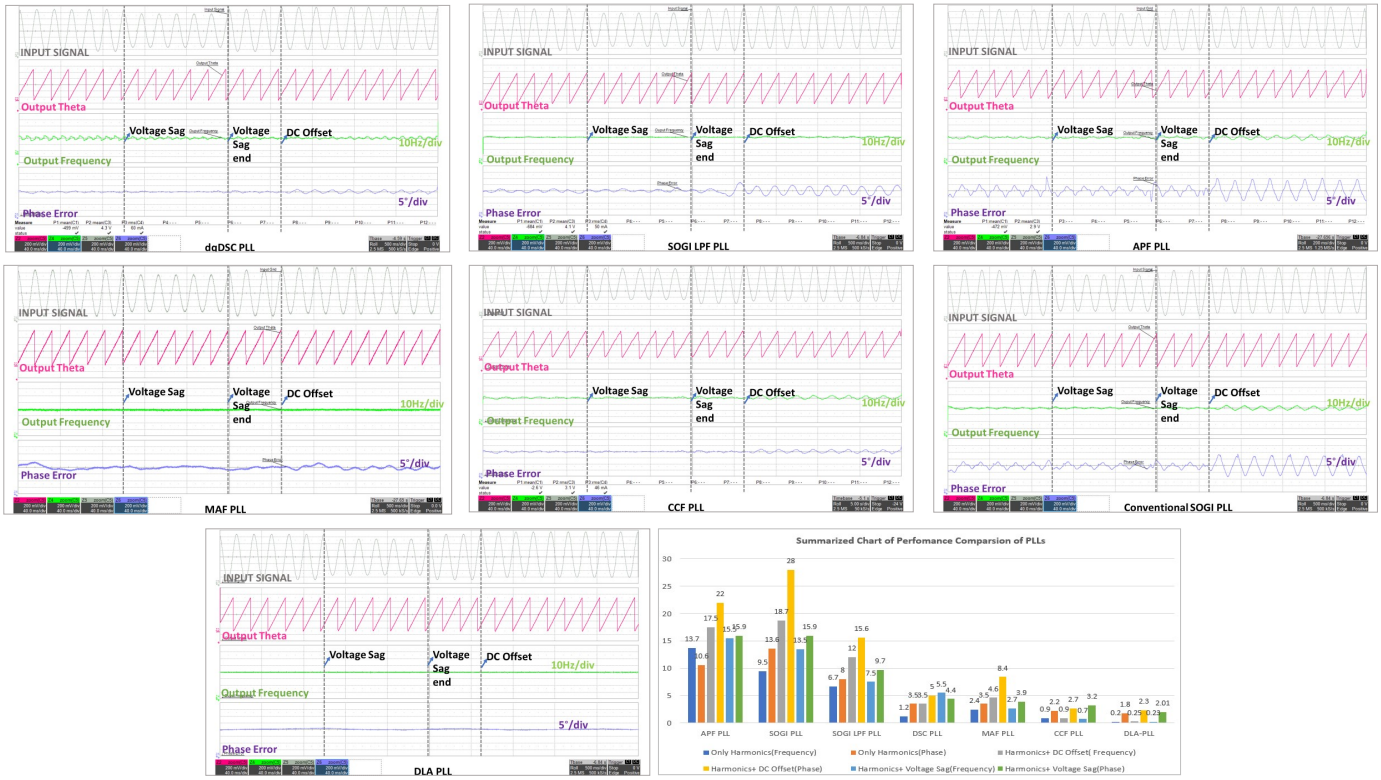


Fig. 3. Experimental results of the proposed techniques and conventional PLLs with distorted grid with voltage sag and DC offset.

clearly shows the distinguished performance in all conditions.

## 3. CONCLUSION

In this paper Digital Lock-In Amplifier PLL is proposed which is compared with six widely used conventional techniques through the simulation and hardware results. Proposed technique shows the frequency variation of 0.32 Hz P-P and 1.2 degrees P-P phase error which completely satisfies the IEEE 1547 standard, even under adverse grid conditions like voltage sag and DC offsets. Proposed technique can prove to be a very useful technique for the power converters to achieve a perfect synchronization with grid in compliance with the grid code and standards.

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