더블라인 주파수 제거를 위한 양방향 컨버터의 전력 디커플링 제어

Power Decoupling Control of the Bidirectional Converter to Eliminate the Double Line Frequency Ripple

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ABSTRACT

In two-stage single-phase inverters, inherent double line frequency component is present at both input and output of the front-end converter. Generally large electrolytic capacitors are required to eliminate the ripple. It is well known that the low frequency ripple shortens the lifespan of the capacitor hence the system reliability. However, the ripple can hardly be eliminated without the hardware combined with an energy storage device or a certain control algorithm. In this paper, a novel power-decoupling control method is proposed to eliminate the double line frequency ripple at the front-end converter of the DC/AC power conversion system. The proposed control algorithm is composed of two loop, ripple rejection loop and average voltage control loop and no extra hardware is required. In addition, it does not require any information from the phase-locked-loop (PLL) of the inverter and hence it is independent of the inverter control. In order to prove the validity and feasibility of the proposed algorithm a 5kW Dual Active Bridge DC/DC converter and a single-phase inverter are implemented, and experimental results are presented.

Index Terms – Dual Active Bridge, Active power decoupling, bidirectional DC-DC Converter, and Ripple rejection

1. INTRODUCTION

The PV systems with single phase AC/DC converters for residential and industrial application need bulky DC link capacitors to eliminate the double line frequency component. Generally, the double line frequency ripple can be reduced with large electrolyte capacitors. Typically, the lifespan of electrolytic capacitors is relatively shorter than those of semiconductor and PV arrays, therefore the reliability of the system also depends on it. To improve the reliability of the system, the electrolyte capacitors needs to be replaced with the film capacitors of which lifespan is quite long. Though the film capacitors have higher ripple current ratings, the ripple has to be minimized by lower system cost. Therefore, it would be better if the ripple can be reduced by the control algorithm such as power decoupling techniques (PDTs). The main concept of PDT is to inject the ripple power to other energy storage components by using external circuit.

In [1] the DC active filters have been proposed to eliminate the input ripple current. In this method, the additional DC chopper circuit is introduced to inject the ripple current. The main drawback of this approach is that it requires an extra switching device and increase the size of system. In another approach [2], the ripple current is reduced by using a current-loop control without using external circuit. However, this technique is not capable of reducing the DC link capacitors. Moreover, it uses a large electrolytic capacitor for the DC link. A method in [3] has realized the DC active filter function without adding extra active devices. It connects the decoupling capacitor to the center tap of the isolation transformer and uses the common-mode voltage to decouple the ripple power. However, this method increases the current rating of the transformer.

To mitigate the ripple power at the DC source side a decoupling capacitor is usually used. The value for the decoupling capacitor (C_D) can be calculated from:

$$C_D = \left(\frac{P_{dc}}{2\pi f_{grid} U_{dc} \Delta u} \right) \tag{1}$$

Where U_{dc} is an average DC voltage across C_D, and Δu is the voltage ripple across C_D. The decoupling capacitance value can be reduced by changing U_{DC} or (and) Δu parameters.

In this paper, the two-loop voltage-feedback controller for the power-decoupling technique is proposed as shown in Fig 1. One loop is for the DC-link ripple elimination, which replaces the current controlled ripple reduction loop. This loop includes a band pass filter (BPF) to reject the DC component of the DC link and bypasses the ripple. PI controller of ripple rejection loop is designed to mitigate the 120-Hz ripple component. The second loop is used to pass the 120-Hz component of the power decoupling capacitor voltage to oscillate around a specified average. The leverage of the proposed control method is that there is no need to have a 120-Hz estimated reference synchronized with the inverter PLL. The proposed controller does not require any information from the inverter circuit hence making it more independent. The proposed DAB circuit has the advantage of a simple single pole, transfer function which makes it more applicable for designing a high-bandwidth ripple rejection control loop. Moreover, the DC link capacitance is effectively reduced by the proposed method.

2. OPERATING PRINCIPLE AND SMALL SIGNAL AVERAGE MODELING

The DAB is a bidirectional DC-DC converter consisting of eight active switches, a high frequency transformer, a leakage inductor and DC-link capacitors as illustrated in Fig. 1(b). Where V_{DC} and V_{DC_link} are the input DC source voltage and output DC-link voltage respectively and L_k is the leakage inductance of the transformer. From the steady state analysis of the DAB converter an equation for the average output power of the converter can be derived as (2).

$$P = V_{dc\_link} I_{P2} = \left(\frac{(1-d)dt V_{dc} V_{dc\_link}}{nL_{lk}} \right) \tag{2}$$

Where 'n' is the turns ratio of the transformer and d is the duty obtained by the phase shift of two bridges, ϕ/π rads.

In order to get the small signal average model of the DAB converter, the equivalent circuit of the converter is derived as shown in Fig.1. It is composed of controlled DC current source, capacitor and resistor connected in parallel with it. The average value of the output current o the DAB I_{P2} is given by;
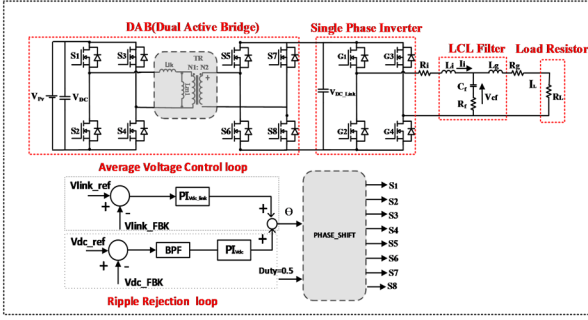
Fig.1. Proposed 2-stage single phase DAB power circuit with control scheme diagram

$$I_{P2} = -\frac{P}{V_{dc\_link}} = \frac{V_{dc}}{n\omega L_k}\phi(1-\frac{|\phi|}{\pi}) \qquad (3)$$

In (3) the negative sign shows the direction of the current. Since, this current source is nonlinear, it should be linearized at the operating point Φ_o for the small signal modeling as shown in (5). Where G_o is the linearized equation of the DAB which can be considered as the gain of the DAB converter where $\omega = 2\pi f_s$ (f_s is the switching frequency).

$$G_o = -\frac{dI_{P2}}{d\phi} = \frac{V_{dc}}{n\omega L_k}(1-2\frac{|\phi|}{\pi}) \qquad (4)$$

$$I'_{P2} = G_o * \phi' = -\frac{V_{dc}}{n\omega L_k}(1-2\frac{|\phi|}{\pi})\ \phi' \qquad (5)$$

In (6) H(s) is the transfer function of the output filter and the load. Where, R_L is the equivalent load resistance, C_{DC_link} is the filter capacitance and $G_c(s)$ represents the PI controller. K is proportional gain and τ is the time constant

$$H(s) = \left(\frac{R_L}{1+C_{DC\_Link}R_L}\right) \qquad (6)$$

$$G_c(s) = K\left(\frac{1+\tau s}{\tau s}\right) \qquad (7)$$

In the small signal modeling, the leakage inductance L_{lk} and the ESR of the capacitor have been neglected to simplify the analysis otherwise the order of the system would be increased. Moreover, the leakage inductance is so small that the pole frequency is usually far above the controller's bandwidth. Therefore, the above-mentioned small signal model is valid in the desired frequency range. With the help of (4) and (6) the transfer functions at each direction can be obtained from the small signal model as followings.

$$Gvdc\_link = \frac{V_{dc\_link}(s)}{\phi} = -Go*H(s) \qquad (8)$$

$$G_{vdc} = \frac{Vdc(s)}{\phi} = -Go*H(s) \qquad (9)$$

4. CONTROLLERS DESIGN

The Proposed power decoupling technique is consisted of two control loops; the first loop is for the (V_{DC}) ripple elimination of DC-source voltage, and the second is to regulate the average voltage across the DC link capacitor to provide the desired RMS voltage required for the inverter output. As explained earlier, one of the advantages of the proposed control technique is that it is sovereign from inverter control and it does not need any information from the second stage inverter.
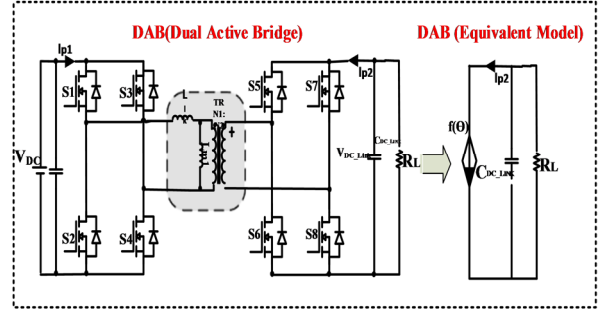

Figure 2 Average model of DAB converter---- a controlled current source

The block diagram of the proposed control loops are shown in Fig.4 (a). In the ripple elimination loop, BPF(s) block is the band pass filter, $PI_{VDC}(s)$ is the PI controller for ripple rejection of the input capacitor, and in the second loop $PI_{VDC\_link}(s)$ is the PI controller for regulating the average voltage across the Dc link capacitor. At first, the ripple elimination loop is designed first while neglecting the effect of average control loop. Then the ripple loop can be omitted as shown in the Fig 4(b). The controller needs to be designed to reject the DC component of DC source capacitor voltage and to have a high gain at 120Hz. Moreover, the ripple rejection control loop can eliminate the ripple component by making the corresponding reference V_{DC_ref} equal to zero. In the ripple rejection loop, center frequency of the BPF is selected by 120 Hz and the value of the damping factor is selected very low to get a higher gain at 120Hz. Thus, the loop gain (T_{VDC}) for the voltage ripple rejection controller can be represented as (10).

$$T_{vdc} = BPF(s) * PI_{vdc} * G_{vdc} \qquad (10)$$

The control loop is designed using MATLAB and the resulting Bode plots is shown in Fig. 3(a). The parameter of the PI controller are Kp = -0.3 and the time constant τ = 10e-3. It can be clearly seen from the Bode plot that the design of the controller has been accomplished as expected. Also, the loop gain is 29.6 dB at 120 Hz, which is adequate to eliminate 120-Hz component from the DC link.

Secondly, the average-voltage controller for DC link voltage is designed using the block diagram shown in Fig. 4(c). The main design consideration for this controller is to allow the 120 Hz AC ripple component of the voltage V_{DC_Link} to freely oscillate around a desired average voltage. Hence, the controller bandwidth is designed to be as low as possible, i.e. less than 120 Hz. In the loop gain design of the average voltage controller, the ripple rejection loop is considered as shown in the block diagram (Fig. 4(c)). The loop gain T_{VDC_link} for average voltage controller is shown as (11), where G_{VDC_link} is the plant transfer function shown in (8) and PI_{VDC_link} is the transfer function of the PI controller.

$$T_{(Vdc\_link)}(s)\Big|_{Vdc\_ref=0} = \frac{PI_{vdc\_link}G_{vdc\_link}}{1+BPF(s)*PI_{vdc}*G_{vdc}} \qquad (11)$$
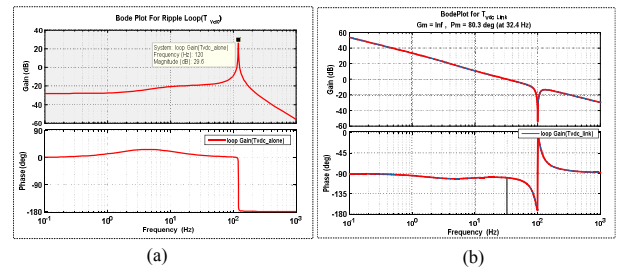

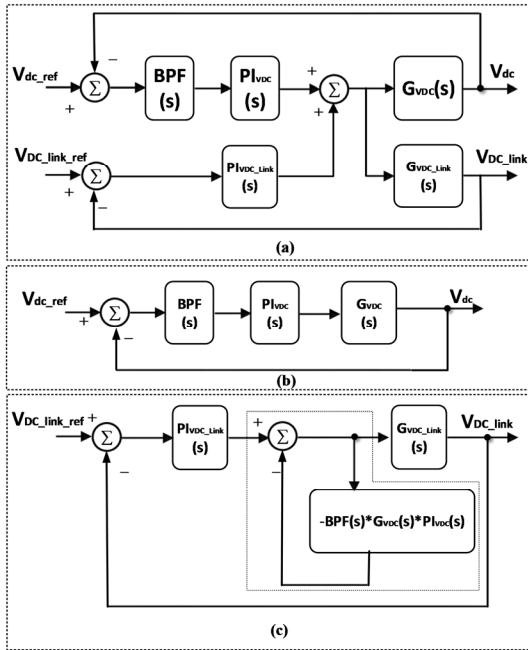Fig. 3. Bode Plot of: a) T_{vdc} b) T_{vdc_link}

Fig. 4. Controlled block Diagram for: a) Proposed DAB control loop for 2-stage converter b) Voltage ripple rejection control loop, neglecting average voltage control loop and c) average control loop and also consider ripple rejection loop.

By using MATLAB, the control designed is performed by the procedure mentioned above. The parameters of the PI controller are tuned with Kp = 0.003 and τ = 30e-3 to achieve the desirable response. Average voltage Controller $T_{VDC\_link}(s)$, has a bandwidth of 32.4Hz and the Phase Margin is 80.3deg. The Bode Plot of loop gain $T_{VDC\_link}(s)$ is shown in Fig. 3 (b).

3. SIMULATION AND EXPERIMENTAL RESULTS

In order to examine the feasibility and effectiveness of proposed power decoupling technique PSIM simulation is performed. The main parameters of the circuit are as followings: C_{DC}=200uF, C_{DC_link}=400uF, Leakage inductance L_{lk}=20.71uH, V_{DC}=380v, V_{DC_link}=400v and 220Vrms as the inverter output. Fig.5 shows the simulation results of the proposed power-decoupling technique at 1kw and 5kw output power.

As observed from simulation results, the voltage on the DC link capacitor has a double line frequency ripple component of 80 V at 5kw. It can be also observed that due to the proposed voltage-control scheme the voltage ripple on the DC source side is successfully reduced with very low capacitance values. The ripple voltage at the DC source capacitor is around 10 V at 5kw, which satisfies the specification of the input voltage of the inverter.

To verify the feasibility of proposed method, a 5kW DAB and a 5kW inverter have been built. Fig.6 illustrates the steady-state experimental results when the proposed decoupling method is enabled. The ripple at the DC source is reduced to 5Vp-p, 9Vp-p, 13Vp-p at 1,2 and 3kw power, respectively though the capacitor values at the DC source is just 200uF and 400uF at the DC link side. The DC link is successfully controlled to maintain 400V for the inverter to make the 220V output. In this experiment film capacitors of which ripple rating is large are used. However, to obtain a similar level of voltage ripple with electrolytic capacitors the DC-link capacitance should be at least 3200μF as
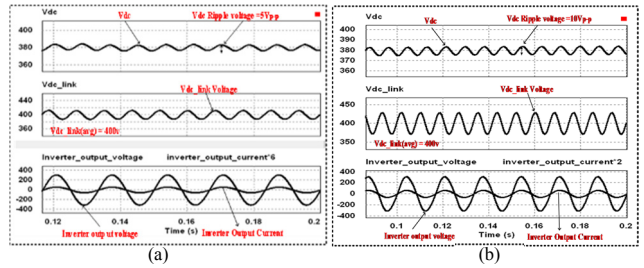

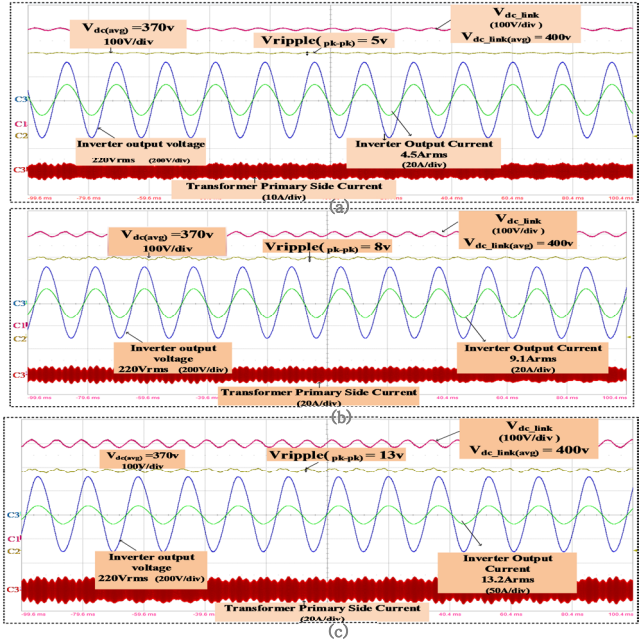Fig. 5. Simulation result of Proposed power decoupling controller (a) 1Kw (b) 5Kw

Fig.6. Steady-state experimental waveforms with ripple power compensation. From top to bottom, dc-link voltage, input capacitor voltage, inverter voltage, inverter current and transformer primary current a) 1kw   b) 2kw   c) 3kw

4. CONCLUSION

This paper has presented a new power decoupling technique for the two-stage single-phase DC-AC power Conversion system. The main advantage of the proposed method is that it does not require additional circuit to reduce the ripple of the converter while successfully attenuating it. Thanks to the ripple reduction capability of the proposed technique the film capacitor can be employed, and the lifespan of the converter system can be extended. In addition, the volume and cost of the converter can be reduced due to the small capacitance value required to maintain the DC link.

5.References

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