Design of 1500V solar inverter stack beyond megawatt in NPC1 topology

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Abstract- This paper describes a design concept of NPC1 power stack for 1500VDC megawatt level solar inverter. This stack uses three latest half-bridge IGBT modules with highest power density and operation junction temperature, which enable realization of power level beyond 1MW without paralleling. Critical design concept on loop inductance is explained. Dynamic characteristics are verified by double-pulse test. Thermal characteristics and output power limits are verified by thermal test. Temperature-sensitive component on PCB as output power constraint is identified. Different PCB repositioning solutions are tested to give the overall output power thermal derating curves, which enable output power of 1.15MW at T_A=55°C with 15°C thermal margin. The power stack characteristic and performance change under different thermal environment is further analyzed.

1. TOPOLOGY AND POWER DEVICE FOR 1500V SOLAR INVERTER

In order to achieve higher power rating and lower system cost, the DC system in solar inverter will increase from 1000VDC bus to 1500VDC bus [1-2]. In higher DC bus voltage, cosmic radiation factor which will increase IGBT field failure rate need to be considered [3]. For this reason, NPC1 topology with 1200V devices as shown in Fig. 1 will be the preferred approach in 1500VDC solar inverter system.

There are two kinds of current commutation loops in NPC1 topology: short commutation loop with active power and long commutation loop with reactive power [4], as shown in Fig.2.

The latest 5th generation of IGBT modules is used to increase power level of inverter, which bring low power losses and high junction operation temperature up to T_{vjop} of 175°C [5-9].

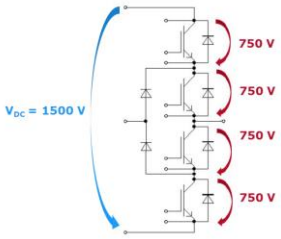


Fig. 1. NPC 1 topology with the expected maximum voltages per switch at DC link voltage of 1500 VDC.

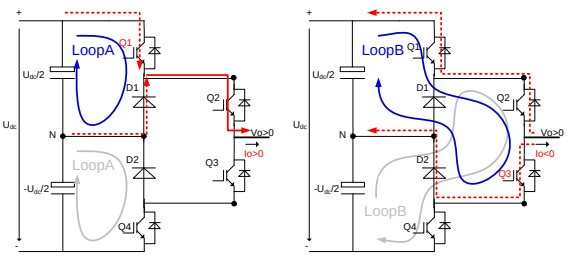


Fig. 2. NPC1 commutation loops: (left) Short loop in active power mode, (right) Long loop in reactive power mode.

2. POWER STAGE DESIGN CONSIDERATIONS

A. *IGBT Module selection*

To construct high-power NPC1 topology, three half bridge modules are needed. IGBT module configuration will influence busbar layout and thus the stray inductance. In this paper, three FF1800R12IE5 half-bridge PrimePACK™ 3+ modules arranged in configuration shown in Fig. 3(a) are chosen for lowest stray inductances.

B. *Busbar design considerations*

Mechanical design of DC and AC busbar influences the overall system structure including cabinet footprint and air cooling system, but it will also affect the compactness of power stack and commutation loops among modules, which defines the stray commutation inductances. Busbar layout and stack design are shown in Fig. 4.

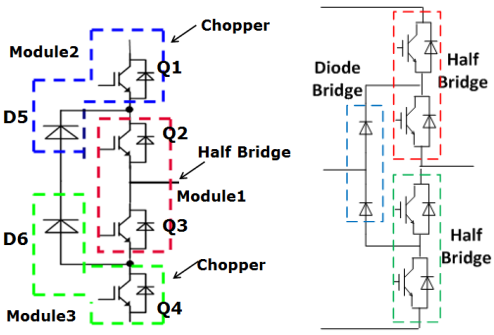
C. *Gate driver design considerations*

The long commutation loop in this stack has high inductance, which brings high VCE turn-off overshoot. To mitigate this overshoot, multi-level turn-off technology is used in gate driver design, in which different R_{goff} are used during turn off process [10]. In NPC1 topology, improper turn off sequence will lead to device over-voltage failure. Proper gate driver design should protect against such turn-off sequence. Fig.4 shows the driver board used in this paper.

3. TEST RESULTS

A. *Electrical Test*

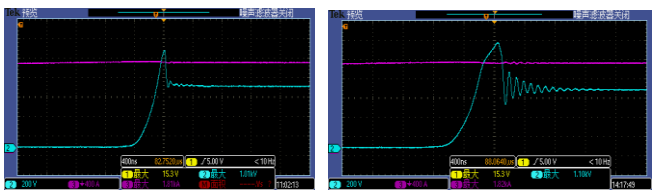
From double pulse test, the short and long commutation loop inductances can be calculated. As shown in Fig.2, there are four commutation loops in one phase. The calculated inductances are 28nH, 115nH, 107nH and 26nH respectively. The inner IGBT Q2, Q3 will have higher turn off VCE overshoot due to higher loop inductance. To reduce VCE overshoot for long commutation loops, one approach is to increase the gate resistor R_{Goff}. Fig. 5 shows the turn-off waveforms of the NPC-1 phase arm with (a) short (VCE1) and (b) long (VCE2) commutation loops respectively with adapted R_{Goff}. The VCE turn-off peak voltages are 1010V and 1100V respectively at rated current. Turn off voltage peak at rated current is close to IGBT rated voltage limit, especially for the inner IGBT with only 100V margin left. To keep IGBT operation within RBSOA, higher turn-off gate resistor for outer IGBT's Q1 & Q4, and multi-level turn-off technique for inner IGBT's Q2 & Q3 are used. Fig. 6 shows the turn off waveforms of inner IGBT's Q2 & Q3 at I_C=3600A. The V_{CE} peak voltage is 976V & 912V, much lower than IGBT V_{CE} rating of 1200V. Fig. 7 shows the short circuit waveforms of top and bottom IGBT of one module. Both top and bottom IGBT's can withstand 7µs short circuit duration, with short circuit currents of 7840A and 9760A respectively. Voltage overshoots for top and bottom IGBT's are 836V and 880V respectively.



(a) (b)

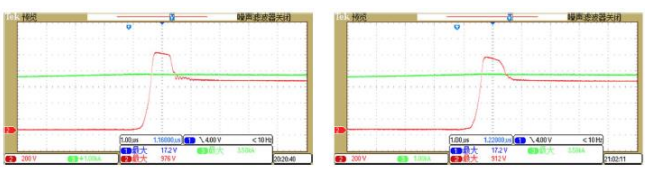
Fig. 3. Construct NPC1 phase arm using PrimePACK modules in (a) Half-bridge and Choppers (b) Half-bridges and Diode bridge configuration.

Fig. 4. NPC1 phase arm design: busbar layout, stack and driver board



(a) (b)

Fig. 5. (a) V_{CE1} Q1 turn off (short loop). R_{Gon}=1Ω, R_{Goff}=1.8Ω and (b) V_{CE2} Q2 turn off (long loop). R_{Gon}=1Ω , R_{Goff}=3.1Ω waveforms for NPC-1 phase arm turn-off. Test conditions: V_{DC}=650V×2, I_C=1800A (rated current), room temperature.



V_{CE-MAX}=976V@3600A V_{CE-MAX}=912V@3600A

Fig. 6. V_{CE} and I_C waveform during Q2 turn off with multi-level turn off. Test conditions: V_{DC}=650V×2, I_C=3600A, room temperature.

B. Thermal Test

In grid-tie solar inverter application, the inverter will generate active power most of the time at power factor close to unity, with current flow through IGBT instead of diode. Conventional full power test using inductive load, with power factor at zero and current flow through diode, is thus not applicable. To verify the thermal performance of stack, DC current source is used to generate the power dissipation P_d in IGBT's (Q1-Q4) and NPC diodes (D5-D6) based on IPOSIM thermal simulation result under full power operation conditions. Convection heating from heatsink to PCB inside cabinet is simulated by covering the whole stack. Thermal test setup and cooling arrangement are shown in Fig. 8. The relationship of stack output power P_O with total power dissipation P_d from all three IGBT modules is shown in Fig. 9. Power dissipation P_d is normalized at P_O=1MW as 100%P_d.

Fig. 7. Short circuit waveform: (left) top IGBT, (right) bottom IGBT. Test conditions: V_{DC}=800V, room temperature. Blue:Vge; Purple:Vce; Green:Isc.

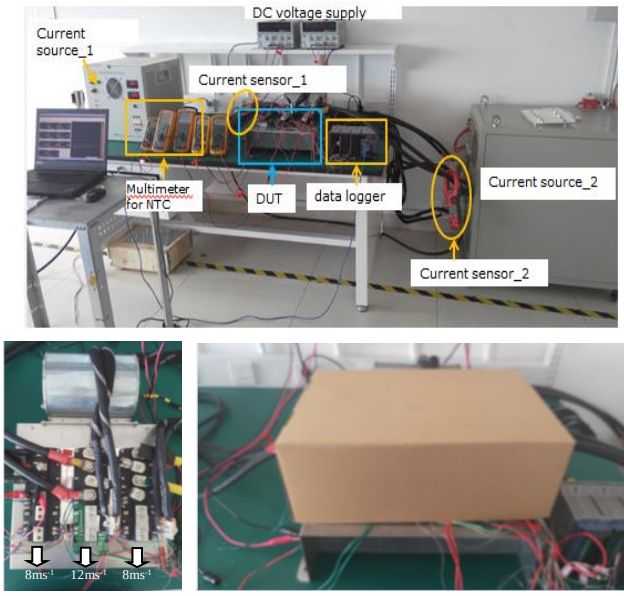


Fig. 8. (Top) Stack thermal test overall setup, (Left) Heatsink and modules, (Right) Stack cover.

Table I shows the power dissipations in IGBTs (Q1-Q4) and NPC diodes (D5-D6), and the results of temperature measurement. The relationships of ΔT_{JA} (P_d), ΔT_{NTC-A} (P_{d_Module}), ΔT_{HA} (P_{d_Total}), ΔT_{NTC-A} (ΔT_{J-A}) and ΔT_{PCB-A} (ΔT_{HA}) are plotted in Fig. 10. Thermal parameters for stack design including thermal resistances R_{thJA}, R_{thCA}, R_{thHA} and temperature correlation factors $\Delta T_{NTC-A}/\Delta T_{J-A}$ and $\Delta T_{PCB-A}/\Delta T_{HA}$ are derived and shown in Table II.

C. Output power constraints and solutions

The maximum output power of stack is not only limited by T_{vjop} of IGBT module, but also by several other thermal constraints including the maximum temperatures of capacitors, IGBT module power terminals, busbars and driver board. For example, the IGBT junction temperature limit T_{vjop} for .XT IGBT5 chip is 175°C, while the max operation temperature of most driver board is only 85°C limited by optical-coupler. From thermal test above, $T_{j,Q1}$ = 128°C and T_{PCB_R} = 57.2°C at 118% of P_d and T_A=31.9°C. At ambient temperature T_A of 60°C, there will still be 19°C margin for $T_{j,Q1}$ while T_{PCB} has already exceeded its limit. This example illustrates that temperature-sensitive components (e.g. optical-coupler in driver board) in the vicinity of high-temperature IGBT module are becoming the bottleneck in the overall thermal design of the power stack. If such thermal bottleneck can be removed, higher output power, higher operating ambient temperature and/or higher thermal margin can be achieved.

Fig.11 shows the stack output power derating with ambient temperature limited by both T_{vjop} of IGBT (red line) and maximum PCB temperature (blue line), with

$\Delta T_{PCB-A}/\Delta T_{HA}$=0.55. Overall power derating is limited by the lower of the two thermal limits as shown by the thick dash line, which gives 115% of P_d at T_A= 60°C for example. If the thermal coupling between PCB and heatsink $\Delta T_{PCB-A}/\Delta T_{HA}$ can be reduced, e.g. from 0.55 to 0.3, output power derating will be reduced as shown by the thin dash line, which allows e.g. 140% of P_d at T_A= 60°C. Thermal coupling between PCB and heatsink can be reduced by forced-air cooling, insulating or re-positioning of the PCB.

New thermal tests were performed to verify the concept above with different PCB re-positioning approaches below:

I. Vertical re-positioning of the PCB

A new PCB (named "Driver Board") is placed 5cm above IGBT module as shown in Fig.12. Temperature rise of PCBs mounted at different positions, together with the stack output power derating with the new "Driver Board" as thermal limit is shown in Fig. 13, which has extended output power range comparing to Fig. 11, e.g. 150% of P_d at T_A = 45°C linearly decreasing to 120% of P_d at T_A = 70°C.

II. Horizontal re-positioning of the PCB

In Fig. 8, the PCB_L and PCB_R are located closed to the heatsink air outlet, which is the hottest part of the heatsink with 17.6°C higher than heatsink air inlet at 141% of Pd. PCB temperature will thus be lower if they are located at the heatsink air inlet.

Fig. 14 shows two PCBs M1 and M2 located at cooling air inlet. PCB temperatures are measured 3cm and 5cm away respectively from IGBT modules. Fig. 15 shows the PCB temperature rises measured at these positions together with the overall stack output power derating with PCB's M1 or M2 as limiting factors, with 15°C thermal margin for both PCB and IGBT from their limits, i.e. maximum operation $T_{j,Q1}$ = 160°C and T_{PCB} =70°C. It can be read from the crossover points in Fig.15 that, the stack can now allow 125% of P_d (equivalent to P_O=1.15MW) at T_A=55°C and P_d derated to 0% at T_A = 70°C, with temperature-critical components located in PCB 5cm from the IGBT module.

If the PCB rating can be upgraded to 105°C, with the same thermal margin of 15°C, maximum operation T_{PCB} =90°C. The stack can further extend its operation range to 100% of P_d (equivalent to P_O=1.0MW) at T_A=78°C, and P_d derated to 0% at T_A= 90°C.

IV. THERMAL ADAPTION ANALYSIS

In this section, the characteristic and output power performance change of the power stack under a new thermal environment is being investigated.

Fig. 16 shows the thermal simulation result of heatsink surface temperature distribution at P_d=120% and T_A=22°C. Q1 has the highest temperature and is the thermal limit of the stack. The thermal resistance of Q1 is decomposed into $R_{thJA,Q1}$ = $R_{thJH,Q1}$ + $R_{thHA,Q1}$ where $R_{thJH,Q1}$ and $R_{thHA,Q1}$ are the thermal resistances per switch of Q1, with heatsink temperature T_H defined as the surface temperature of heatsink directly under the chip.

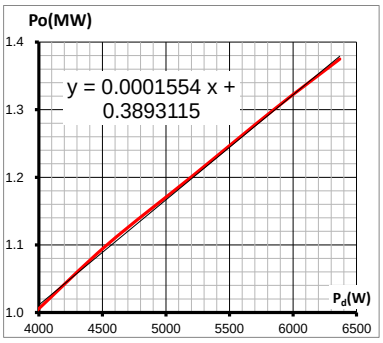


Fig. 9. Stack output power P_O with total power dissipation P_d from all three IGBT modules.

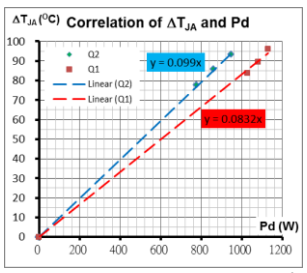
TABLE I. TEST CONDITIONS AND TEMPERATURE MEASUREMENT RESULTS

Pd (W)	Q1	Q2	Q3	Q4	D5	D6	$T_{j,Q1}$	$T_{j,Q2}$
100%	1028	780	780	992	461	461	115.4	109.4
109%	1081	864	864	1041	525	525	121.4	117.6
118%	1130	948	948	1092	604	604	128.0	125.2

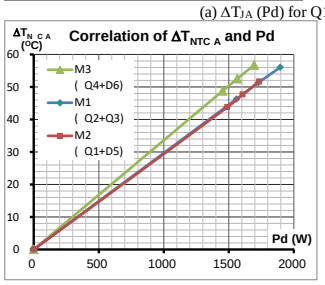
T_NTC1	T_NTC2	T_NTC3	H1	H2	H3	PCB_L	PCB_R	In
78.0	75.5	80.5	70.5	56.4	65.0	49.1	52.8	31.7
83.1	79.5	84.4	74.3	58.5	67.7	51.0	54.7	31.8
87.9	83.6	88.7	77.8	61.2	70.7	52.8	57.2	31.9

TABLE II. THERMAL RESISTANCES AND CORRELATION FACTORS

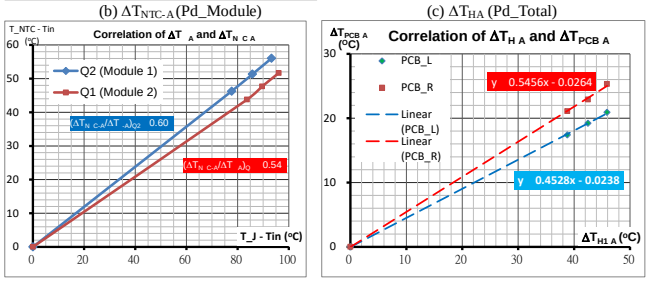
K/kW	R_{thJA}	R_{THCA}		R_{thHA}		$\Delta T_{NTC-A}/\Delta T_{J-A}$		$\Delta T_{PCB-A}/\Delta T_{H1-A}$	
Q2	99	Module 3	33.5	H1	8.6	Q1	0.54	PCB_R	0.545
Q1	83	Module 1	29.6	H2	5.5	Q2	0.6	PCB L	0.452
D6	162	Module 2	29.8	H3	7.3	D6	0.63		



(a) ΔT_{JA} (Pd) for Q1, Q2 (left) and D6 (right)



(b) ΔT_{NTC-A} (Pd_Module) (c) ΔT_{HA} (Pd_Total)



(d) ΔT_{NTC-A} (ΔT_{J-A}) (e) ΔT_{PCB-A} (ΔT_{HA})

Fig. 10. Relationships amongst different temperature measurements.

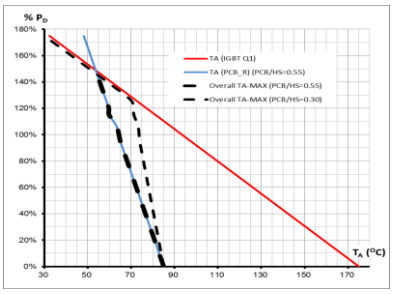


Fig. 11. Stack output power thermal derating by IGBT module and PCB temperature limits.

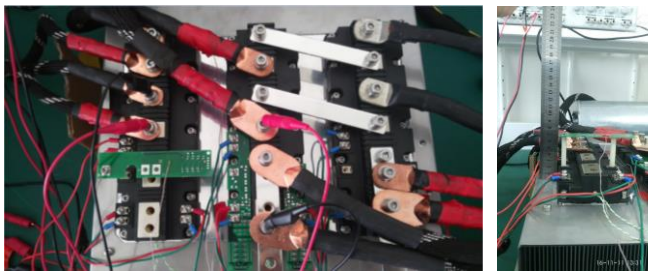


Fig. 12. New PCB "Driver Board" placed 5cm over IGBT module

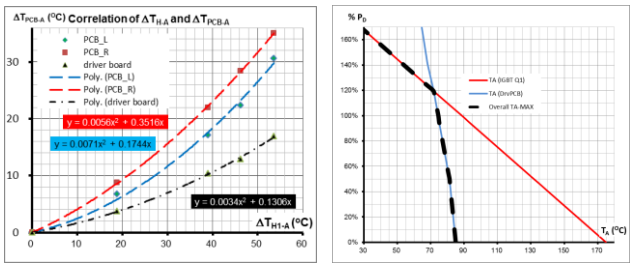


Fig. 13. (a) PCB temperature rise at different positions. "Driver Board" is mounted 5cm over IGBT module. (b) output power derating.

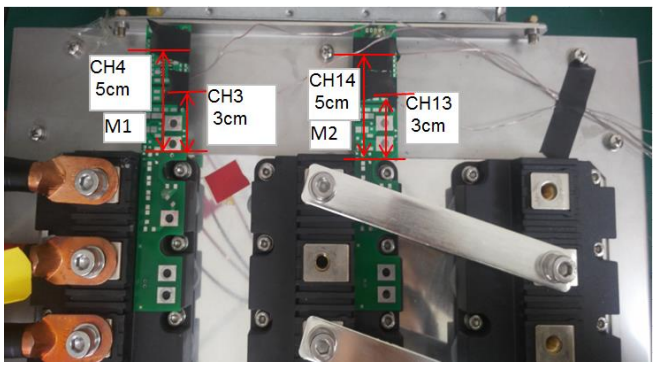
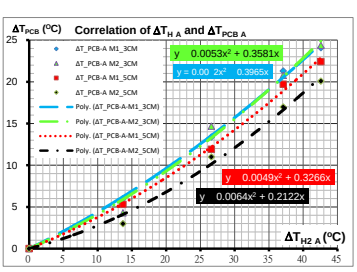


Fig.14 New PCBs M1 and M2 located at cooling air inlet, with temperatures measured 3cm and 5cm respectively from IGBT modules.



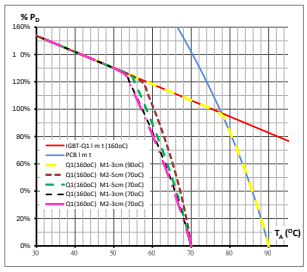


Fig.15. (a) PCB temperature rise at different positions from cooling air inlet, (b) Stack output power derating with PCB mounted at cooling air inlet.

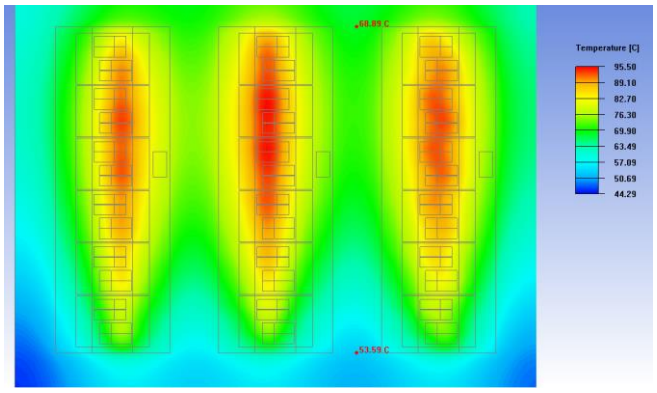


Fig.16. Thermal simulation result of heatsink surface temperature distribution at P_d=120% and T_A=22 C.

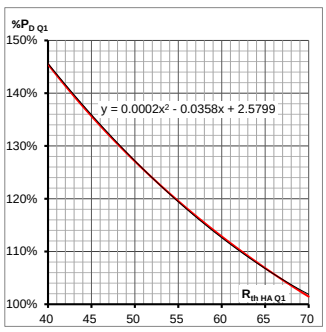


Fig.17. Stack output power as function of heatsink thermal resistance $R_{thHA,Q1}$, at T_A = 55 C and 15 C margin for Q1 from T_{vjmax}.

The average heatsink temperature for Q1 ($T_{H,Q1}$) can be estimated from simulation result as around 86°C. Thermal resistance $R_{thHA,Q1}$ is estimated to be 51.9K/kW by $(T_{H,Q1}-T_A)/P_{d\_Q1}=(86-22)/(1.2\times1028)$. With $R_{thJA,Q1}$=83.2 K/kW, $R_{thJH,Q1}$ =31.3 K/kW.

In actual design, the heatsink thermal resistance $R_{thHA,Q1}$ is subjected to changes due to different heatsink dimensions and/or fan being used. Moreover, the cooling air velocity may also be reduced due to fan wear out or dust accumulation in air channel. With $T_{j,Q1}$ as the thermal limit, 15°C margin from $T_{vjmax,Q1}$, and T_A = 55°C, the relationship of maximum stack output power with heatsink thermal resistance is shown in Fig.17, with P_d=100% equivalent to Po=1.0MW

V. SUMMARY AND CONCLUSION

To realize NPC1 topology in 1500VDC bus solar inverter, three half bridge IGBT modules can be used. The latest chip and package technologies bring the highest power density at high operation temperature. The busbar, gate driver and thermal design are important design considerations.

Temperature-sensitive PCB components in the vicinity of IGBT module can be the bottleneck of power stack thermal design. Output power derating can be improved by re-positioning of PCB vertically or horizontally, which enable the output power of 1.15MW (125% of P_d) at T_A= 55°C while keeping 15°C thermal margin for IGBT and PCB.

Thermal characteristics of stack are dependent on the heatsink thermal resistance $R_{thHA,Q1}$ which is subjected to changes. Design curve to correlate output power with R_{thHA} is derived.

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