3-레벨 NPC 인버터에서 보조 레그를 이용한 공통 모드 전압 제거

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Cancellation of Common-Mode Voltages in Three-Level NPC Inverters with Auxiliary Leg

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ABSTRACT

In this paper, a new active circuit for common-mode voltage (CMV) cancellation in three-level NPC (neutral-point clamped) inverters is proposed, which can avoid the saturation of the common-mode transformer (CMT). The proposed circuit utilizes an additional three-level leg to produce the compensating CMV of the NPC inverters, which eliminates the CMV of the inverter through the CMT.

1. Introduction

Nowadays, the reduction of the CMV in the NPC inverters is an important issue since the high power machine drives are widely utilized in industrial applications [1]–[3]. Therefore, the CMV of the inverter, which leads to leakage current through stray capacitors, bearing current, shaft voltage and motor winding-to-ground voltages, should be reduced or eliminated to maintain the life-time of the motors and transformers [3]–[7]. The methods based on the external circuit using the complementary symmetry transistors [4], [5], are inappropriate for the medium voltage application. Another external circuit for the CMV elimination applicable to the medium voltage class was suggested in [7], but this method utilizes the full-bridge circuit, which can cause the saturation in the CMT if an asymmetric ON period of the switches exists. The saturation of the CMT causes a high primary current, which may result in the damage the switching devices and CMT.

This paper presents an active circuit, which cancels the CMV of the three-level NPC inverter. With an auxiliary leg to produce the compensating voltage, the CMV of the inverter can be eliminated. In addition, the saturation of the CMT can be avoided by the half-bridge circuit.

2. CMV Elimination of Three-level NPC Inverters

2.1 CMV of NPC inverters

The 3-level NPC inverter consists of two capacitors for DC-link and four active switches and two clamped diodes for each phase leg as shown in Fig. 1(a). For the regular SVPWM, all 27 voltage vectors are utilized, as shown in Fig. 1(b).

The CMV of the NPC inverters, which is defined as the voltage between the neutral point of the load and the mid-point of the DC-link, is expressed as

$$v_{CMV} = v_{nO} = \frac{v_{AO} + v_{BO} + v_{CO}}{3} \quad (1).$$

Therefore, the CMV of the NPC inverters with the regular seven-segment switching pattern varies among five voltage levels such as $-V_{dc}/3$, $-V_{dc}/6$, 0, $V_{dc}/6$ and $V_{dc}/3$, where the voltage step is $V_{dc}/6$.

2.2 Existing method for CMV cancelation

An active circuit with a full-bridge circuit of IGBT was proposed to compensate the CMV of the NPC to overcome the power and voltage rating limitation of the external circuit as shown in Fig. 2 [7]. This method can successfully cancel the

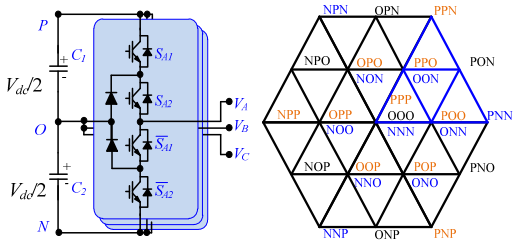


Fig. 1. Three-phase three-level NPC inverters. (a) Circuit. (b) Space voltage vector diagram.

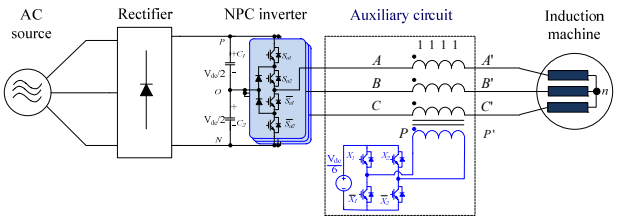


Fig. 2. Induction motor drive system with the auxiliary circuit for CMV elimination [7].

CMV of the NPC inverter with the combination of the modified SVPWM, which can reduce the CMV of the inverter to three voltage levels of $-V_{dc}/6$, 0, and $V_{dc}/6$ by utilizing 19 voltage vectors as shown in Fig. 3. Then, the additional full-bridge circuit generates the compensating voltage with three-level, which is the same of CMV. Therefore, the CMV of the NPC inverter can be eliminated fully. However, the structure of the external full-bridge circuit can lead to the saturation of CMT in practical implementation due to asymmetrical operating condition.

3. Proposed Circuit for CMV Elimination

3.1 Structure of the external circuit

The proposed circuit is composed of an auxiliary leg of the NPC inverter and two small capacitors C_{X1} and C_{X2} as shown in Fig. 4. The auxiliary leg can generate three voltage levels of $V_{dc}/2$, 0, and $-V_{dc}/2$. By the CMT turn ratio of 3:1:1:1, the compensating voltage on the secondary windings varies among $V_{dc}/6$, 0 and $-V_{dc}/6$, which can eliminate the CMV.

For control of the auxiliary leg, both gating signals, g_{X1} and g_{X2}, are OFF if the inverter CMV is $-V_{dc}/6$ and are ON if it is $V_{dc}/6$. When the CMV is *0*, the gating signal of g_{X1} is OFF while g_{X2} is ON. Due to the structure of the half-bridge, the DC component of current cannot flow into the mid-point of the C_{X1} and C_{X2}. Therefore, the saturation does not occur in the CMT even though there is an unsymmetrical operating condition.

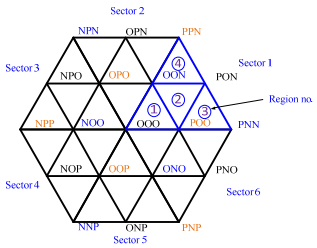


Fig. 3. Modified SVPWM utilizing only nineteen voltage vectors for three-level NPC inverter

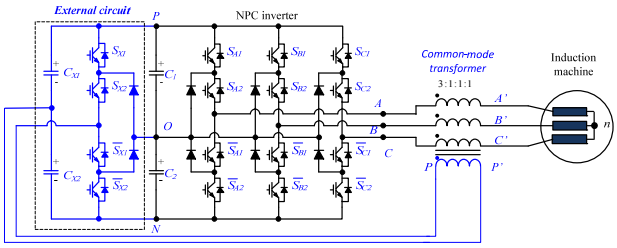


Fig. 4. Proposed circuit for CMV cancelation with additional leg.

4. Simulation Results

The simulation results for medium-voltage high-power application with PSIM software were carried out to verify the effectiveness of the proposed method. The simulation conditions are listed in Table I.

Fig. 5 shows the effectiveness of the proposed method for CMV elimination, where the auxiliary leg is activated at t=0.1s. Fig. 5(a) shows the line-to-line voltage of the inverter. Fig. 5(b) shows the three phase currents of the inverter, which are unchanged for two periods. Fig. 5(a) and (b) show that the proposed method does not affect the output performance of the inverter. Fig. 5(c) and (d) show the compensating and CMV voltages, respectively, where during the first duration when the auxiliary circuit is not activated, no compensating voltage is produced, so that the CMV varies in three voltage levels of 1,083 V, 0 V, and -1,083 V. For the next duration when the auxiliary leg is activated, the compensating voltages are generated, so the CMV of the inverter is fully cancelled.

Fig. 6 shows the ability of the proposed circuit to avoid the CMT saturation, where the gating signal has an asymmetry with a longer ON duration of 0.4 %. The parameters of the CMT are listed in TABLE II. In these operating conditions, the full-bridge circuit generates the DC offset component, which also causes the offset component in transformer flux as shown in Fig. 6(a_1) and the high primary current of about 200 A due to the saturation effect as shown in Fig. 6(a_3). To the contrary, the proposed half-bridge circuit does not produce any offset component in the primary winding of the CMT. Therefore, no saturation exists as shown in Fig. 6(b). The flux of the CMT varies around the zero value as shown in Fig. 6(b_1) and the CMT magnetizing current is kept low as shown in Fig. 6(b_3), of which peak value is below 2 A.

5. Conclusions

This paper has proposed the CMV elimination circuit with an auxiliary leg of the NPC inverter, which can successfully apply to the high-power medium-voltage applications. With the half-bridge structure, the saturation of the CMT due to different unsymmetrical conditions can be avoided.

TABLE I. SIMULATION PARAMETERS OF HPMV NPC INVERTERS

Parameters	Value	Parameters	Value
DC-input voltage	6,500 V	Rated output frequency	60 Hz
DC-link capacitance	3,000 μF	Rated output voltage	4,160 V
Switching frequency	2,000 Hz	Rated output power	2.0 MW

TABLE II. CMT PARAMETERS

Parameters	Value	Parameters	Value
Number of turns	42:14:14:14	Effective cross section	0.03 m^2
Inductance factor	260 H/$turn^2$	Saturation flux density	1 2 T

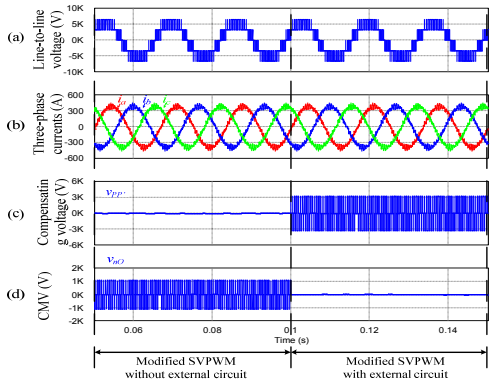
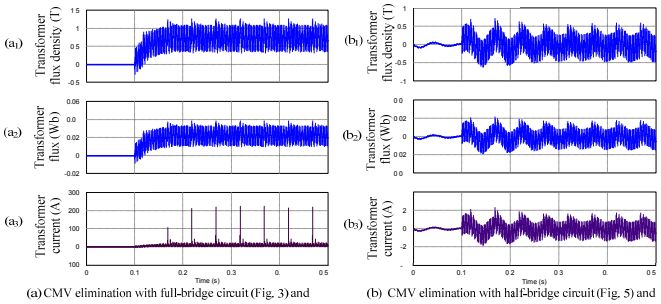


Fig. 5. CMV elimination ability of the proposed method



(a) CMV elimination with full-bridge circuit (Fig. 3) and mismatch control

(b) CMV elimination with half-bridge circuit (Fig. 5) and mismatch control

Fig. 6. Desaturation ability of the proposed circuit

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