중전압 응용을 위한 새로운 하이브리드 5-레벨 인버터

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A Novel Hybrid Five-Level Inverter for Medium-Voltage Applications

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ABSTRACT

This paper proposes a new hybrid five-level voltage-source inverter topology, based on the conventional five-level active neutral-point-clamped topology (5L-ANPC), where the lower number of switching devices is required, resulting in saving the cost. The operating principle and control method of the proposed topology is described. The comparison of THD, power losses, loss distribution, and cost of components are evaluated among the proposed topology, the 5L-ANPC and 5L-DCI (diode-clamped inverters) topology.

1. Introduction

Nowadays, multilevel converters have become a favored choice for medium voltage and high power applications due to attractive advantages such as lower dv/dt output voltage, lower total harmonic distortion (THD), better voltage and current waveform and higher voltage capability [1]. In recent years, five-level topologies have gained an increasing attention not only in the academia but also in the industry since they can offer better performance compared with three-level topologies whereas the cost is reasonable due to the decrease in the price of high voltage, high power IGBT modules. The issue of complex control requirement for five-level converters can also be overcome by the virtue of the availability of high performance DSP (digital signal processors).

In this paper, a new hybrid five-level voltage source inverter (5L-HI) is proposed based on the 5L-ANPC topology. The proposed topology has two advantages over the 5L-ANPC. The first is that a lower number of switching devices are required, thus its cost is reduced. Secondly, the proposed topology has a better distribution of power losses. The only drawback of the proposed 5L-HI is that the DC-link capacitor voltages cannot be balanced with a diode front-end rectifier. However, this problem can be overcome in back-to-back systems without any constraints on the operation of both inverters and converters [2]. Since the 5L-ANPC has been successfully commercialized by ABB [3], its topology is used for comparison with the proposed topology in term of THD, power losses and total component cost. To make it general, the comparison also includes the 5L-DCI topology.

2. Proposed 5L-HI Topology and Control

2.1 Structure of the proposed 5L-HI

A simple single-phase diagram of the proposed topology, as shown in Fig. 1, consists of eight switching devices, one flying capacitor and three capacitors for common DC-link. To achieve the five-level output voltage waveform, the voltage of each capacitor must be pre-charged and kept at specific values that are one fourth of V_{DC} for the flying capacitor, the upper and lower DC-link capacitors, and a half of V_{DC} for the middle DC-link capacitor. Eight switches can be divided into three units as Cell 1, Cell 2 and Cell 3. The devices of Cell 1 and Cell 3 have the same voltage rating of $V_{DC}/4$, but the devices of Cell 3 have a double value, which means a half of V_{DC}. If two series-connected

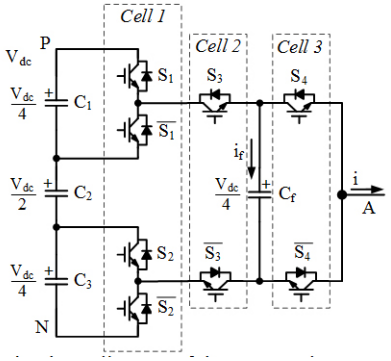

Fig. 1. Single-phase diagram of the proposed 5L-HI.

Table I. Switching states of the proposed 5L-HI with effects on the voltages of C_f and C_2

S1	S2	S3	S4	VAN	Switching states	Effect on V_{C_f}		Effect on V_{C_2}	
						i>0	i<0	i>0	i<0
0	0	0	0	0	V_0	0	0	0	0
0	1	0	0	$V_{DC}/4$	V_1	0	0	+	−
0	1	0	1	$V_{DC}/2$	V_2	−	+	+	−
0	1	1	0	$V_{DC}/2$	V_3	+	−	−	+
0	1	1	1	$3V_{DC}/4$	V_4	0	0	−	+
1	1	1	1	V_{DC}	V_5	0	0	0	0

IGBTs are used for Cell 2, total 10 equally-rated switches are needed for each phase leg.

2.2 General operation

To generate five output voltage levels for each phase, six switching states are used. The pairs of switches, $(S_1, \overline{S_1})$, $(S_2, \overline{S_2})$, $(S_3, \overline{S_3})$ and $(S_4, \overline{S_4})$, are operated in a complementary way. For simplicity, only the states of four switches, S_1, S_2, S_3 and S_4, are listed in Table I, where the on and off states of each switch are indicated by "1" and "0", respectively. Table I also shows the effects of each switching state on the voltages of the flying capacitor V_{C_f} and the middle DC-link capacitor, V_{C_2}.

The voltage of the flying capacitor can be balanced independently and maintained through two redundant switching states for $V_{DC}/2$, which are V_2 and V_3, that can charge and discharge the flying capacitor based on the direction of the phase output current. To determine which switching state needs to be applied, a simple signal can be used as defined in (1). If the polarity of SG_x is positive, then the switching state V_2 would be used, whereas V_3 would be used if SG_x is negative.

$$SG_x = (v_{f\_x} - V_{DC}/4) i_x \quad (1)$$

where v_{f_x} and i_x are the flying capacitor voltage and the measured current of phase x, respectively.

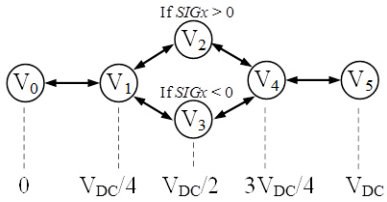

Fig. 2. Recommended transitions for the proposed 5L-HI.

Table II. Parameters of simulation model

Parameters	Values
Power Rating	1.3 MVA
Output Voltage	2.3 kV
Input DC Voltage	3.6 kV
Output frequency	60 Hz
Carrier frequency	2000 Hz
Flying capacitors	1000 µF
Output Inductance	4 mH

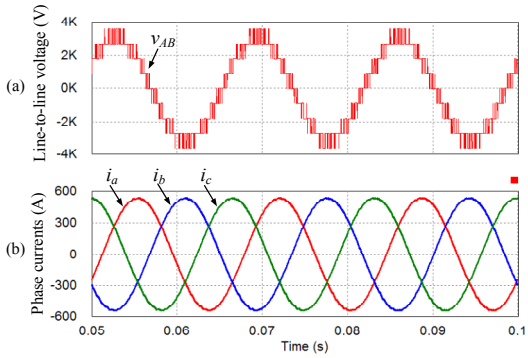

Fig. 3. Voltage and current waveforms at unity modulation index (MI = 1). (a) Line-to-line voltage. (b) Phase current.

In order to achieve smooth transitions between output voltage levels as well as to minimize switching losses, the switching states should be selected as recommended in Fig. 2. It can be noticed that the commutation between V_2 and V_3 should be avoided since it requires more switching steps that leads to higher switching losses.

2.3 Simulation Results

In order to verify the operation and performance of the proposed 5L-HI, a 1.3MVA/2.3kV inverter has been designed and simulated using PSIM. For simplicity, the DC-link capacitors are replaced with ideal voltage sources. The parameters of the simulation model are shown in Table II.

Fig.3 shows the performance of the proposed inverter using sinusoidal PWM (at unity modulation index) with four level-shifted carrier signals. The THD value of the line-to-line output voltage is about 17%, which is similar to that of 5L-ANPC and 5L-DCI topology with the same modulation technique.

3. Evaluation of Power Losses and Costs

A simplified model for three topologies (5L-HI, 5L-ANPC and 5L-DCI) is designed and simulated with parameters listed in Table II. For simplicity, a three-phase ideal sinusoidal current source (peak value 600A) is used as a load. IGBT FF450R17IE4 is chosen for all models. All the inverters are controlled by a same modulation technique, which is a sinusoidal PWM (carrier frequency is 2 kHz).

Fig. 4 shows the power loss comparison of three inverters with different modulation indexes at unity power factor. It can be seen

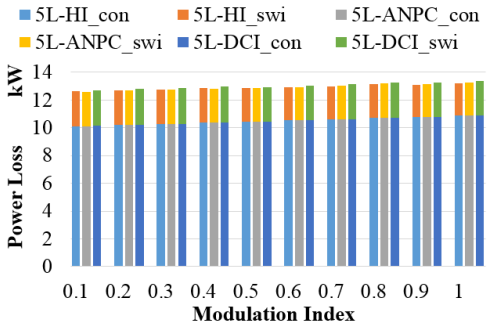

Fig. 4. Power loss comparison at various MIs ($\cos\varphi = 1$).

Table III. Cost Comparison (in USD)

Devices	5L-HI		5L-ANPC		5L-DCI	
	no.	Price	no.	Price	no.	Price
Dual Switch: FF450R17IE4	15	4,500	18	5,400	12	3,600
Clamped diode: DD600N18K	0	0	0	0	18	2,250
Capacitor: B25620B1158K103	7	1,540	7	1,540	4	880
Gate driver: 2SD315AI	15	1,350	18	1,620	12	1,080
Summation		**7,390**		**8,560**		**7,810**

that the difference of power losses between these inverters is insignificant.

To evaluate the costs of three-phase 2.3-kV, 1.3-MVA inverters with 5LHI, 5L-ANPC, and 5L-DCI topologies, only the costs of IGBT devices, gating drivers, diodes and capacitors are taken into account. Table III lists the number of devices and the costs for three topologies.

In the proposed 5L-HI topology, the inverter has the lowest number of devices, resulting in the lowest cost. The cost of the proposed 5L-HI is reduced by **13.7%** and **5.4%** compared with that of 5L-ANPC and 5L-DCI, respectively.

4. Conclusions

This paper has presented a new five-level hybrid inverter topology for medium-voltage high-power applications. The proposed topology has been compared with 5L-ANPC and 5L-DCI topology in term of performance, THD, power losses and device costs. The evaluation results show that the proposed topology gives a similar performance as that of the existing topologies whereas the number of components and thus the cost and size are reduced considerably.

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