Comparison study of the future logic device candidates for under 7nm era

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HP (Year of production = 2021, Lg = 9.7nm)			
EOT (nm)	Vdd (V)	*Ion (uA/um)*	*Ioff (nA/um)*
0.59	0.64	1,976	100
LSTP (Year of production = 2021, Lg = 10.2nm)			
EOT (nm)	Vdd (V)	*Ion (uA/um)*	*Ion (pA/um)*
0.8	0.63	572	10

Table
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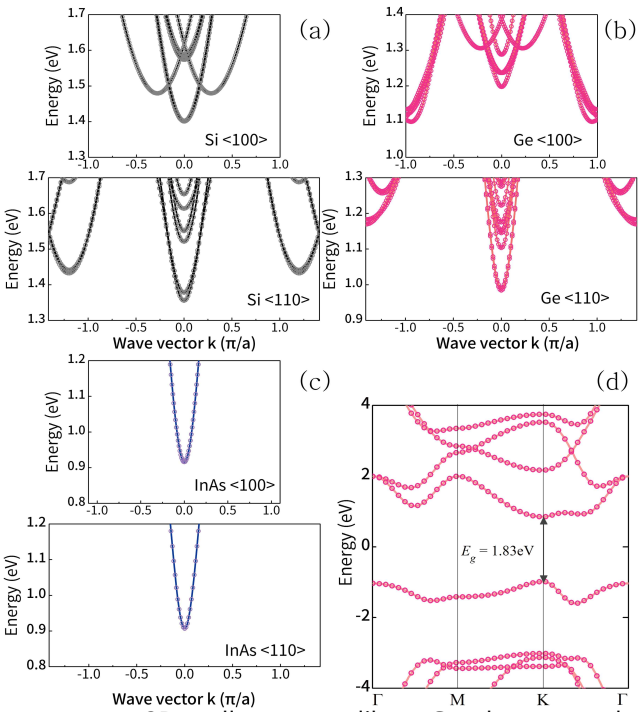
Future logic device over the FinFET generation requires a complete electrostatics and transport characteristic for low-power and high-speed operation as extremely scaled devices. Silicon, Germanium and III-V based nanowire-based MOSFET devices and few-layer TMDC (Transition metal dichalcogenide monolayers) based multi-gate devices have been brought attention from device engineers due to those excellent electrostatic and novel device characteristic. In this study, we simulated ultrascaled Si/Ge/InAs gate-all-around nanowire MOSFET and MoS2 TMDC based DG MOSFET and TFET device by tight-binding NEGF method. As a result, we can find promising candidates of the future logic device of each channel material and device structures.

INTRODUCTION

CMOS scaling technology leads a revolution in informatics and electronics over 40 years [1]. Traditional scaling theory depends on Denard's scaling theory until several dozens of nanometer technical nodes [2], but nowadays scaling requires a different and fundamental shift in device structure and physics. Short channel effect leads traditional planar devices to the multi-gate device since the early 2010s. Leading manufacturers introduced tri-gate structure multi-gate(MG) based MOS structure, well known as FinFET device to continue device scaling and improve channel performance of the transistor. [3] The FinFET structure is virtually state-of-art design scheme for nowadays logic devices. It is expected that FinFET based structure hold position late 2010 to early 2020 years, as known as 10nm technical node level. ITRS report predicts that gate length will be scaled near the 10nm gate length (L_G) when early 2020 years. [4] Moreover, MOSFET reveals the beginning of the 2020s, device engineers call it as 7nm or 5nm technical nodes. (or N7 and N5) For achieving this drastic scaling, GAA (Gate-all-around) nanowire structure have been expected novel device for future CMOS generation due to its perfect electrostatics in the channel region. [5] Especially, non-Si based channel material like Germanium (Ge) or Indium Arsenide (InAs) has been anticipated because of those novel carrier transport characteristic as the channel material. [6] Another promising candidate is a two-dimensional material based electronic device. Two-dimensional electron devices take the spotlight lately, Because of a novel characteristic of 2D semiconductor materials, such as Van der Waals dangling bond-free surface, uniform thickness, parasitic degradation effect free channel, and good electron transport property. 2D allotropes like Graphene and Phosphorene or TMDC is a typical example. Especially, MoS2 (Molybdenum disulfide) is one of most promising material for next-generation nanoelectronic device [7].



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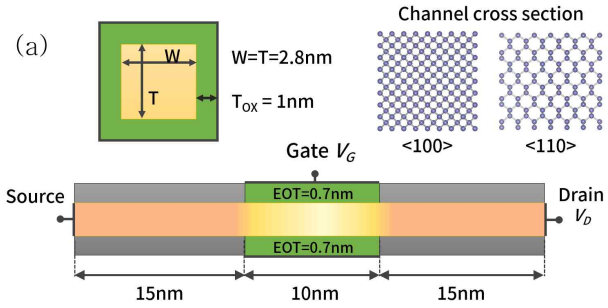
In this study, we target device as following ITRS 2012 roadmap [4], which is shown in Table 1. L_G=10nm device which is expected early 2020 years. Moreover, the device structure of MOSFET is GAA(gate-all-around) nanowire structure and DG(Double-gate) structure for 2D semiconductor MoS2 device. Moreover, we also simulated tunneling based transport scheme for MoS2 DG structure by change doping parameters of each device.

CALCULATION METHODS

To evaluate the basic I-V characteristics of each device, which is strictly according to quantum effect including atomistic full-band information, we ran atomistic effective-band self-consistent ballistic quantum transport simulation using $sp^3d^5s^*$ and sp^3s^* tight binding model [8][9] and non-equilibrium Green's function (NEGF) transport method using by

EDISON Tight-binding NEGF numerical solver.



(b)

S/D Doping Concentration (cm^{-3})			
Si	Ge	InAs	MoS_2
1e20	1e20	2e19 5e19	1e21 5e20

RBT (Reduced basis Transformation) method is used to reduced massive size Hamiltonian, which is calculated from the full-band atomistic tight binding calculation of several hundred to of channel atoms. All calculations set as unstrained NW structure, same as the bulk lattice constant for each material.

Full-band atomistic $sp^3d^5s^*$ tight-binding calculation performed for determining E-k band structure of extremely scaled nanowire structure and Energy band structure for Brillouin zone of single layer MoS2 structure. The calculations were conducted by EDISON Tight-binding band structure calculation S/W.

RESULTS AND DISCUSSION

1. Band structure effect on extremely scaled nanowire structure.

According to preceding research, ultra-scaled semiconductor suffers quantum confinement effects [11]. Bandstructure effects in strongly quantized semiconductor structure reveal as transformed subband structure and electronic band gap (Eg) of semiconductor material. [12].

Fig. 1 shows the E-k diagram from the $sp^3d^5s^*$ tight-binding calculation for each semiconductor nanowire and Monolayer MoS2 structure. Optimal channel material can deliver huge amount charge during channel operation. In this respect, Lighter effective mass (m*) at the edge of conduction and high DOS (density of state) for near conduction band (E_C) are key factor of maximize channel current. For Si nanowires (Fig. 2(a)), both <100> and <110> channel direction NW have minimum subband at k=0 points. There are multiple bands at each the lowest subband edge point, which means that those have high DOS. However, relative round conduction band edge comparing with InAs and Ge NW means that those have relative heavy effective mass (m*). It implies that SiNW has high DOS and low injection velocity (v_{inj}) in NW channel. On the other hand, InAs NW has the contrary characteristic to SiNW. InAs NW has single subband at k=0 points with lighter m* which means high v_{inj}. However, the single conduction subband minimum edge is represented as low DOS in NW channel region in both InAs <100> and <110> NW. In between two channel direction, <110> InAs NW has slightly lighter m*. For the Ge <110> NW, there is m* lighter than Si NWs. Moreover, multiple conduction subbands at lowest point mean that it has higher DOS than InAs NWs, so we can obtain Ge <110> NW as one of the best candidate for GAA nanowire FET device. However, Ge <100> NW has heavier effective mass than Ge <110> NW. Figure (d) is full band structure of 2H-MoS2. It has a gradual change in subband energy near lowest subband region, so we expect MoS2 has relatively heavier m* than other materials.

The quantum confinement effect in electronic bandgap also can deduct from the $sp^3d^5s^*$ tight-binding calculation. In Fig 2, we can see each the lowest conduction subband energy edge higher than bulk band gap (E_g). The practical value of extremely-scale (Width and Thickness matched for 2.8nm) rectangular GAA NW is in Table 2. In this table, each NW has even higher E_g than the bulk parameter. Another interesting facts is NWs E_g differ from transform direction, because of each <100> and <110> NW has different confinement direction ([010]/[001] for <100> NW and [-110]/[001]) and surface density of atoms. In the case of Ge and InAs NW, Each semiconductor has increased factor more than two times than bulk one. These results correspond with the previous researches for extremely confined semiconductor structure [11][12][13].

Figure 2. (a) is Simulated device (GAA nanowire FET) structural diagram. For MoS_2 TMD device, channel and source/drain region convert to single layer 2H-MoS_2 semiconductor. (b) is doping concentration properties of each channel materials.

2. Device simulation and result.

Fig. 2 depicts test devices of the simulation. Using parameter of ITRS 2012 roadmap which is presented in Table. 1, Parameter are set as EOT (Equivalent Oxide Thickness) is 0.7nm, the gate length (Lg) is 10nm, and Source and drain length are equally 15nm, and fixed drain voltage (VD) is 0.6V. For MoS2 DG device, channel convert to single layer 2H-MoS2 and The transport direction is Zigzag direction.

Table 2. The electronic band gap of Bulk semiconductors and ultra-scaled nanowire structure.

Other parameters are same as GAA NW device.

Fig. 3(a) show simulation results of drain current (I_D) for a gate voltage (V_G) sweep for Si, Ge, and InAs GAA NW NFET (N-type NFET) device. All simulation result, the threshold voltage (V_{th}) shifted for static 100nA/um

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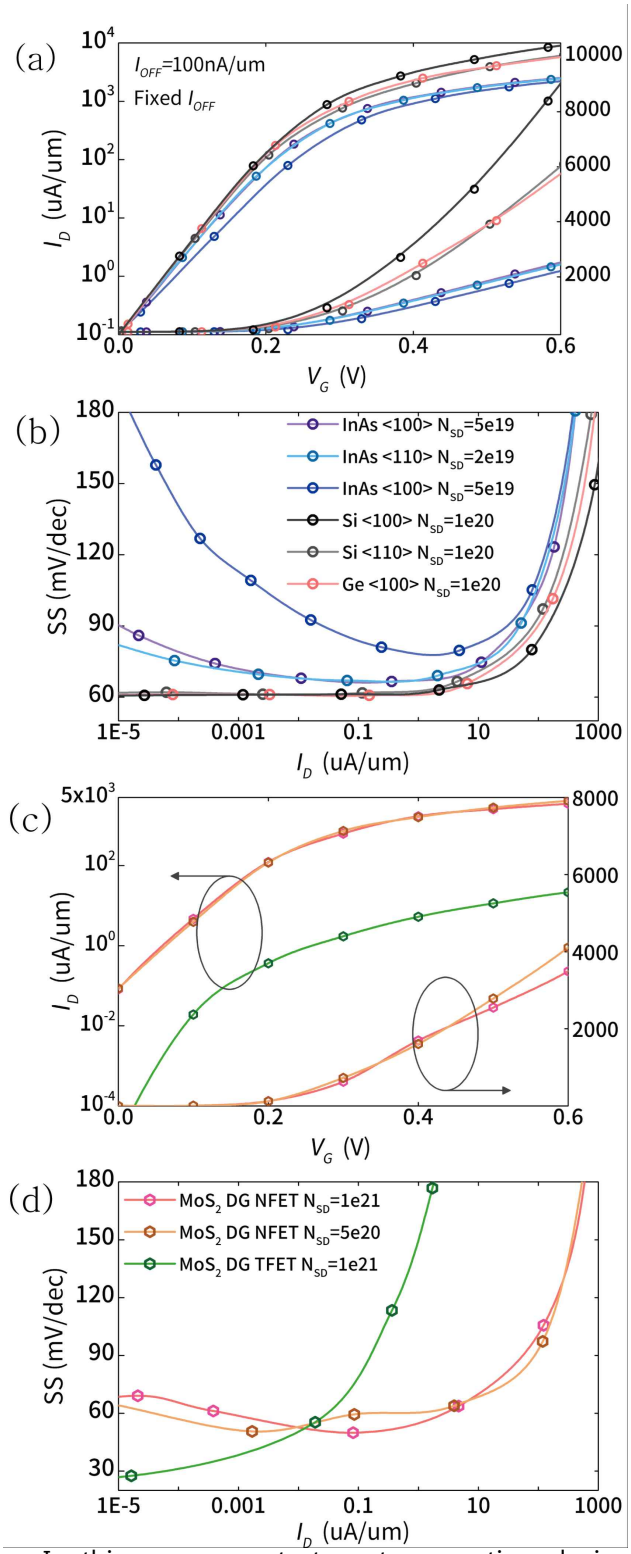
off-current (I_{OFF}) of HP guideline of Table 1. The normalized current conversion of channel width follows the generalized equivalent DG MOSFET model [14]. Moreover, device supply voltage (V_{DD} = 0.6V). The current plot is a linear sweep of static drain bias voltage (V_D) and increasing gate bias voltage (V_G). First of all, all of the simulated devices easily satisfy on current level (I_{ON}) of ITRS roadmap [4] of ballistic transport mode of nanowire device. The current levels at V_D=V_G=0.6V excess 2,000uA/um, so it can deal with possible candidate future logic device of 7nm and under the technical node. The both InAs <110> and <100> NW devices have lower than Si and Ge NW device due to low DOS, despite light m* of conduction band which is previously referred to in E-k diagram of NW structure in Figure 1. Simulation result of Si <100>, Si <110> and Ge <100> NW has optimal current level due to high DOS and relative light m*, so much higher drive current than InAs NW. Fig 4(b) is subthreshold slope (SS) of each device. Especially Si <100> and Ge <100> NWs are most prominent characteristic for all channel choices, both I_{ON} and SS characteristic. Doping concentration of source/drain region significantly effects on channel SS characteristic. In Si and Ge NW case, SS is near ideal (~60mV/dec) for thermionic emission phenomena. In the case of InAs <110> NW, optimization of channel doping is critical to channel SS. Heavily doped case (N_{SD}=5e19) have poor SS characteristic in the low current window, but optimized channel doped device (N_{SD}=2e19) have relative moderates SS (<90mV/dec). Ideal SS device (in the case, Si and Ge NW) can expect to convert to LSTP device by Vth shifting and additional device parameter optimization. Si and Ge GAA NW devices have drastic current increasing near threshold voltage (see Fig 3(b)), So It is another clue that Si and Ge NW devices are a proper candidate for LSTP device.

Fig 3(c) and (d) is simulation result of MoS_2 TMD device. Similar to GAA NW device, MoS2 DG FET device also expects outstanding on-current (I_{ON}) characteristic and SS. The I_{ON} near operating voltage V_D is parallel to GAA NW device of figure 3(a). The SS of MoS_2 NFET device also have a theoretical value near 60mV/dec, So MoS2 NFET device is also optimal to both HP and LSTP device. In the case of tunneling based FET device, which is implemented as p-i-n doping structure. It has sub-thermionic SS characteristic (<60mV/dec) in the subthreshold current region. So this device is expected as a very low standby current device, but shown in Fig 3(c), I_{ON} of TFET has significantly low then it comparing with the NFET device. Additional structural and parametric optimization required for evolution to high-speed operation TFET device.

CONCLUSION



In this paper, we test next generation device candidates by atomistic and ballistic simulation by EDISON TB-NEGF solver. The result presented Si, Ge, InAs based GAA NW FET and MoS2 DG FET device is the relevant nominee for the future Lg=10nm device as ITRS projection of early 2020. Si <100> NW transport direction have best ballistic current in comparison with Ge and InAs NW transport channel. Moreover, In the case of InAs NW FET device, optimal source-drain doping is a crucial factor of short-channel GAA NW FET design. MoS_2 DG

FET device is also a mighty candidate for the future logic device.

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