Potential Model for L shaped Tunnel Field−Effect−Transistor

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Abstract

A surface potential model is introduced for L-shaped tunnel field-effect-transistor (L-TFET). Excellent agreement is obtained when model results are compared with TCAD data.

Index Terms

Band-to-band-tunneling, compact model, surface potential, tunnel field-effect-transistor (TFET)

I. INTRODUCTION

Tunnel field-effect-transistor (TFET) has recently attracted considerable attention as a potential replacement to conventional complementary metal-oxide-semiconductor technology (CMOS).

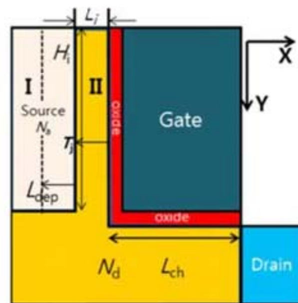

Fig. 1. Schematic of L-TFET.

TFETs have been demonstrated to achieve a much lower SS as compared to conventional MOSFET [1]. However, their ON current performance has not been exhibited to match conventional MOSFET. Recently, an L-shaped vertical TFET (L-TFET) [2] has been introduced as shown in Fig. 1. L-TFET comprises of a heavily doped source and drain regions, and an intrinsic channel. The channel in an L-TFET comprises of 2 sections. One is a tunneling region sandwiched between source and gate dielectric where tunneling takes place. The other part of channel is where transport takes place and is found under the gate dielectric as highlighted in Figure 1.

II. SYSTEM MODEL AND METHOD

In an L-TFET, potential is constant in the tunneling region. Therefore, 1-D Poisson equations are solved in both regions I (source) and II (intrinsic channel) [3]. In order to solve Poisson equation, electron concentration was ignored.

Solution of Poisson equation in region I integrated between x=T_j and x=L_{dep} is given by,

$$\frac{L_A^2}{2}\left[\frac{E_j^2}{V_{th}^2}\right] = \exp\left(-\frac{\varphi_j}{V_{th}}\right) + \frac{\varphi_j}{V_{th}} - 1 \quad (1)$$

Solution of Poisson equation in region II integrated between x=T_j and x=0 (at surface) is given by,

$$\frac{L_A^2}{2}\left[\frac{E_j^2}{V_{th}^2}\right] = \exp\left(-\frac{\varphi_j}{V_{th}}\right) - \exp\left(-\frac{\varphi_s}{V_{th}}\right) + \frac{N_D}{V_{th}N_A}[\varphi_j - \varphi_s] \quad (2)$$

Since both potential and electric field must be constant at x=T_j, (1) and (2) can be compared at x= T_j to obtain junction potential φ_j, whereas, surface potential φ_s can be obtained by expressing depletion length L_{dep} of region I as a function of φ_s.

Junction potential φ_j can be found from the following equation.

$$\varphi_j = V_{th} - V_{th}\exp\left(-\frac{\varphi_s}{V_{th}}\right) + \frac{N_D}{N_A}\varphi_s + \frac{L_A^2}{2}\left[\frac{E_s^2}{V_{th}^2}\right] \quad (3)$$

Figure 2(a) and (b) show surface potential results obtained from the model compared with surface potential obtained from TCAD for 2 L-TFET devices dimensions of which are mentioned in Table 2.

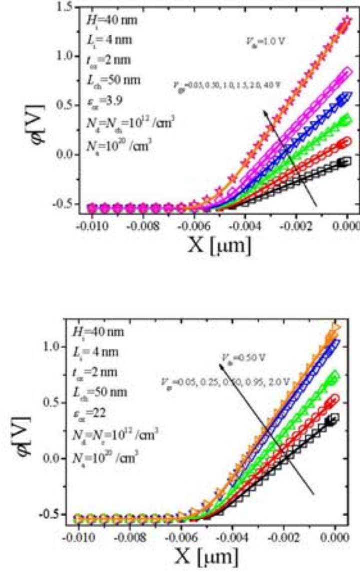

Fig. 2. (a) and (b) potential profile along channel in the tunneling region for different V_{gs} and V_{ds} values for device 1 and 2, respectively. Lines: model, symbols: TCAD.

IV. CONCLUSION

Excellent agreement is obtained between TCAD results and surface potential obtained from the model. This potential model can be used to calculate the shortest tunneling distance from which Ids – V_{gs}, and I_{ds} – V_{ds} relationship can be evaluated.

Table 1. Symbols- their meaning and units

Symbol	Quantity	Unit
L_A	Extrinsic Debye length	cm
q	Charge on an electron	Coulomb
E_j	Junction/surface electric field	V/cm
E_s	Surface electric field	V/cm
V_{th}	Thermal voltage	V
φ_s	Surface potential	V
N_D/N_A	Donor/Acceptor conc.	/cm^3
T_j	Junction thickness	nm
L_{dep}	Depletion length	nm
H_i/L_i $/L_{ch}$	Height/length of insulator region, and length of channel	nm
t_{ox}	Dielectric thickness	nm
$\varepsilon_{ox}/\varepsilon_{si}$	Oxide/silicon permittivity	F/cm

Table 2. Device dimensions for devices used

Symbol	Device 1	Device 2
H_i	40 nm	40 nm
L_i	4 nm	4 nm
t_{ox}	2 nm	2 nm
L_{ch}	50 nm	50 nm
N_d/N_a	10^{12} / 10^{20}	10^{12} / 10^{20}
ε_{ox}	3.9	22

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