무작위와 체계적인 것에 의한 지터를 제어하는 지연고정루프

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A Random and Systematic Jitter Suppressed DLL

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요 약

무작위와 체계적인 것에 의한 지터를 제어하는 지연고정 루프가 소개 되었다. AC는 연속적인 지연 단의 지연 시간을 평균화 하고 모든 지연 단의 지연시간을 동일하게 한다. 지연위상고정을 기반으로 한 0.18um CMOS공정으로 제작된 클럭 발생기의 측정결과는 13.4ps rms 지터 크기를 보였다.

ABSTRACT

A random and systematic jitter suppressed DLL is presented. The AC averages the delay time of successive delay stages and equalizes the delay time of all delay stages. Measurement results of the DLL-based clock generator fabricated in a one-poly six-metal 0.18μm CMOS process shows 13.4-ps rms jitter.

키워드

delay locked loop, average circuit

Ⅰ. Introduction

DLLs are often used in clock multiplication and, recently, greater emphasis is being placed on suppressing jitter in clock signals as the speed of modern chips rapidly increases. The combination of a PLL with a recirculating DLL is used to generate a high frequency and low jitter clock signal but it requires a clean reference signal and complicated circuits [1]. A DLL with a divider and a VCO-like VCDL is used for frequency multiplication. The VCDL includes a MUX which selects the reference signal or the VCDL output signal [2]. In this paper, an AC is introduced in [3] to suppress the systematic and random jitter among the delay stage in the VCDL. Moreover, a capacitor with a switch working effectively as a negative feedback function is introduced to the loop filter to further suppress jitter. It has been implemented in a 0.18μm CMOS process to verify the proposed DLL-based clock generator.

Ⅱ. Architecture of the dll with Averaging circuit

The entire architecture of the proposed DLL-based clock generator with an AC is shown in Fig. 1. It consists of a phase detector (PD), a charge pump (CP), a loop filter (LF), a voltage controlled delay line (VCDL), a delay variance voltage converter (DVVC), an averaging circuit (AC), and a frequency multiplier (FM). The VCDL in Fig. 2 is made of ten differential delay stages and each delay stage is negative feedback looped with an AC. Each delay stage has two input signals from LF and AC. V_n, V_k and V_{cn} are the output signals of VCDL, DVVC and AC, respectively.
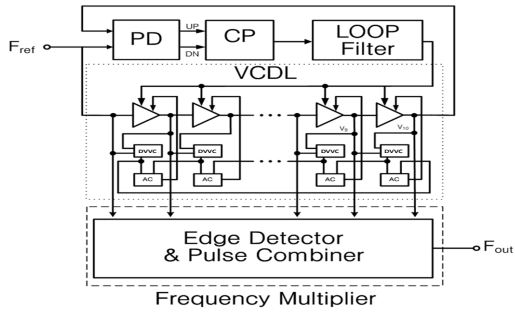
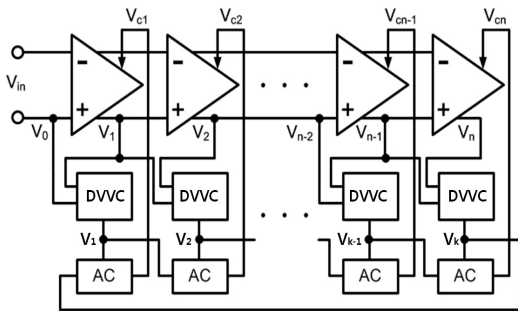Fig. 1. Block diagram of the proposed DLL-based clock generator.

Fig. 2. Block diagram of the proposed VCDL. The VCDL is negative feedback looped with a DVVC and an AC.

The main negative feedback loop consists of the PD, CP, LF and the VCDL. The output voltage of the LF is from the main negative feedback loop and is used to control the delay time of the whole VCDL. The additional negative feedback loop consists of one delay stage in the VCDL and AC. The DVVC senses the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the systematic and random delay variance of each delay stage in the VCDL.
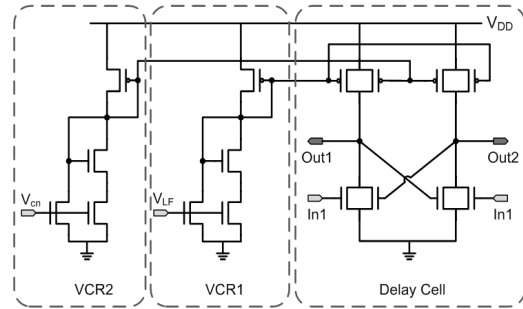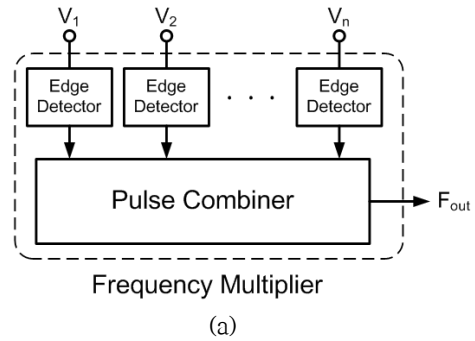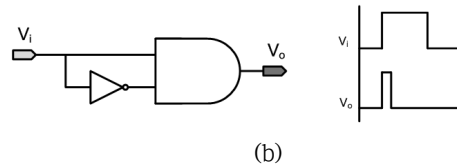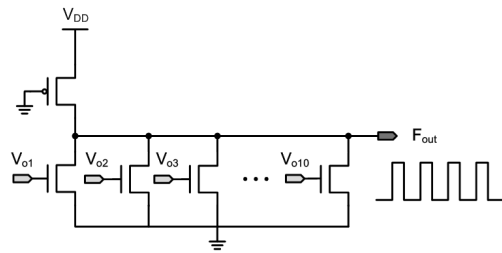
III. Circuit description

Fig. 3. Circuit diagram of voltage controlled resistor & delay stage.

Fig. 4. (a) Frequency Multiplier, (b) Edge Detector, (c) Pulse Combiner.

Fig. 3 shows the delay stage used in the VCDL. Each delay stage has two voltage controlled resistors (VCR) which convert the output voltage from the LF (V_{LPF}) and the DVVC(V_{cn}) into a current to control the delay time of each delay stage. Fig.4 shows the frequency multiplier which consists of an edge detector and pulse combiner. The edge detector consists of an
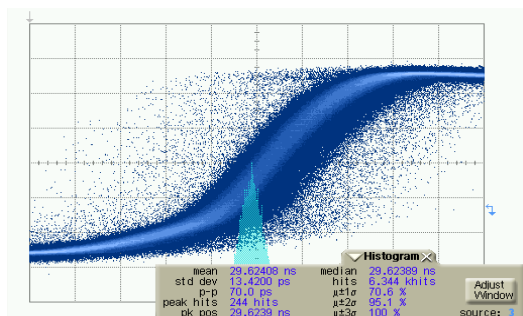
inverter and AND gate that generates a pulse signal when its input signal rises. The pulse combiner combines those pulses to generate a high frequency output signal.
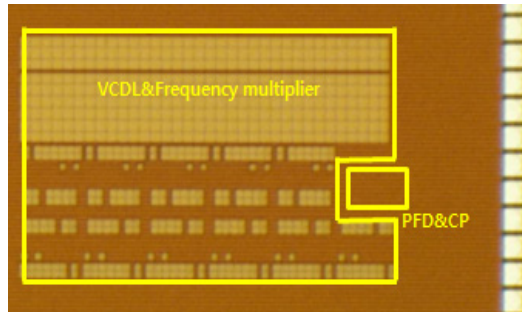
(a)
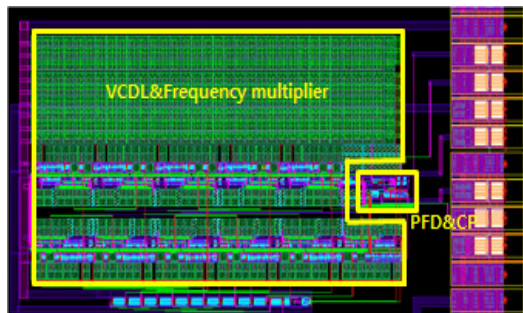
(b)

(c)

Fig. 5. Measurement results of the DLL. (a) Chip photograph, (b) layout of DLL, and (c) jitter characteristic at 500MHz.

Ⅳ. measurement results

The proposed DLL was implemented using a one-poly six-metal 0.18 μm CMOS process. The chip photographs, layouts and measured jitter characteristics are shown in Fig. 5. The lower layers of transistors and capacitors are not seen because of the thick multi-inter-metal layers. The die area is 1110 μm * 730 μm in Fig. 5 without LF capacitors.
The measured multiplied output clock signal has 13.4-ps rms jitter.

Ⅴ. Conclusion

This paper suggests that using a DLL-based clock generator with an AC in the VCDL can suppress both random and systematic jitter. The DVVCs and ACs form a negative feedback loop in the VCDL. The DVVC senses the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the random and systematic delay variance of each delay stage in the VCDL.

References

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