

Tile Level Rate Control for High Efficiency Video Coding (HEVC) on Multi-core Platform

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Abstract

This paper proposes a tile level rate control for High Efficiency Video Coding (HEVC). The proposed tile level rate control is designed by considering the multi-core platform of tile in HEVC. The proposed tile level rate control allocates the number of bits for each tile based on the predetermined weight generated from the current picture level rate control. According to the experimental results, the proposed tile level rate control for HEVC on multi-core platform loses negligibly the bitrate accuracy about 0.07% on average over the reference software HM-14.0.

Keywords: High efficiency video coding (HEVC), R-lambda model, rate control, tile, multi-core platform, video coding

1. Introduction

The existence of rate control algorithm is very essential for video encoder. It takes into account the encoder to meet the bandwidth and the resource requirement while maintaining the video quality. Rate control also ensures overflow and underflow prevention of the buffers in decoders. Considering the importance of rate control algorithm, some predecessors of video codecs already included the rate control algorithm into the reference software which adjust the rate control algorithms based on the quantization parameter (QP) adaptively [1]. As a new generation of video coding standard, High Efficiency Video Coding (HEVC) [2], has also studied several rate control models during the Joint Collaborative Team on Video Coding (JCT-VC) meetings [3, 4]. And the R-Lambda model rate control is now integrated for the reference software HEVC test Model (HM) [5].

In general, R-Lambda model in HEVC, including the mostly rate control algorithms in video coding, allocates some number of bits into different coding levels consisting group of pictures (GOP) level, frame level, and coding block unit level (CTU). In order to achieve the target bit, some video source parameters are then estimated (e.g., mode, motion, and quantization parameter). These parameters play important roles in any rate control algorithm affecting on the output bitrate of the coded video.

Due to the increased market demand of video with high resolution (e.g., Ultra High Definition (UHD) video sequence), HEVC introduces Tile for the parallelism tool. Nowadays, tile has been widely used as one of parallelization tools to accelerate the encoding or decoding process. It is performed by partitioning a picture into a number of rectangular regions without any data dependencies among the partitioned regions. However, overlap threading process might usually occur in the multithreading of tile level. It may lead the abnormally changing of the encoder output bits. And practically, it will interfere the video quality even worse. If a rate control algorithm is also performed in tile level, this abnormally changing of bits can be prevented. However, the current rate control of HEVC does not consider yet the tile level rate control. Therefore, this paper is proposed to investigate the tile level rate control for HEVC by considering the multi-core platform functionality of tile.

As reminder, this paper is organized as follows. In Section II, we describe the proposed algorithm for HEVC. In Section III, the

performance evaluation of the proposed algorithm is discussed. Finally, we conclude our work briefly in Section IV.

2. The Proposed Tile Level Rate Control

As described in Section I, HEVC has integrated the R-Lambda model rate control into the reference software HM. This model is designed by considering the relationship between rate and distortion expressed as:

$$D(R) = CR^{-K} \quad (1)$$

where D is distortion estimated by MSE (Mean Square Error), R is the rate in pixel-based (bpp), C and K are the model parameters. Therefore, the slope of the $D(R)$ curve can be generated as:

$$\lambda = -\frac{\partial D}{\partial R} = CK \times R^{-K-1} = \alpha \times R^\beta \quad (2)$$

Where α and β are the video source parameters updated during encoding of each CTU. The best Lambda for the current CTU is computed before encoding based on the target bits estimation.

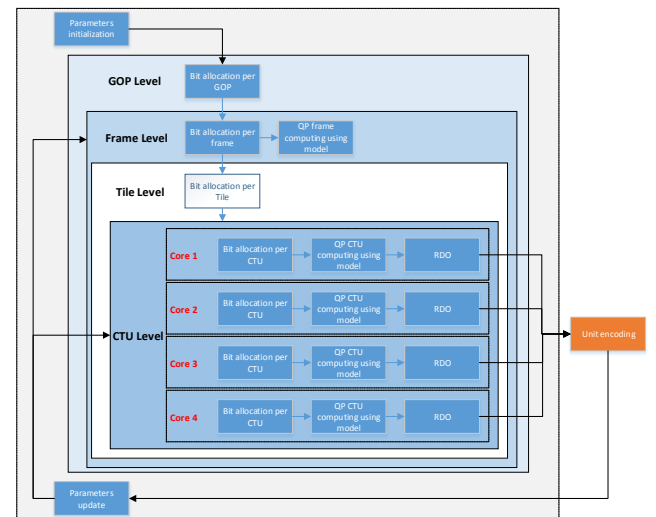


Fig. 1. Block-diagram of the proposed tile level rate control

In our work, the way to allocate bits for GOP level, picture level, and CTU level is the same with the current rate control framework. And our proposed tile level rate control also uses similar schemes for the bit allocation in each tile. The bits allocation of each tile is based on the predetermined weight from the current picture level rate control. Assume that the target bitrate of a picture is already estimated. Then the target bit of the current tile is determined likely in CTU level of the current rate control framework. And then, the CTU level rate control is performed under the multi-core platform of tile level as shown in Figure 1 and Figure 2. Figure 1 presents the block-diagram of the proposed tile level rate control and Figure 2 shows the CTU level rate control performed in multi-core platform of each tile.

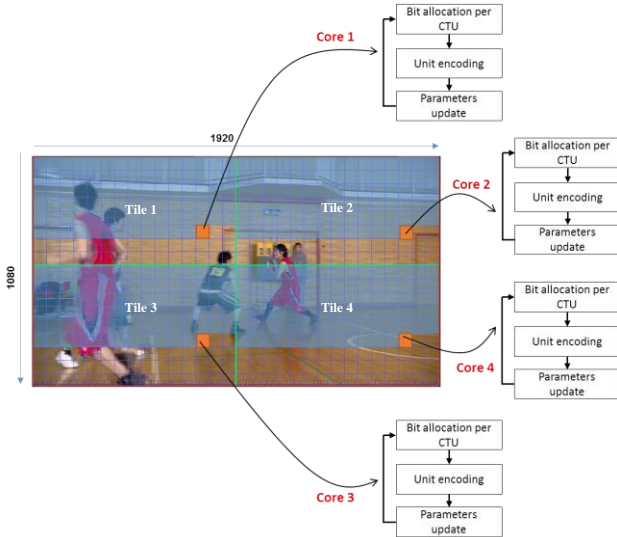


Fig. 2. Multi-core platform of tile and CTU level rate control

3. Experimental Results

For performance evaluation, video sequences of Class A and B were used in random access mode under the common test condition of JCT-VC. The experimental results were evaluated on Windows 7 (64-bits) OS over 3.30GHz quad core with 16GB RAM. Table I is the experiment results of the proposed algorithm, compared to those of the reference software of HM-14.0.

The performance evaluation is conducted with 4 tile partitions to meet the target bitrate in approximation 30 Mbps. The accuracy bitrate is calculated as:

$$acc = \left(1 - \frac{|TB - AB|}{TB}\right) \times 100(\%) \quad (3)$$

where TB denotes the target bitrate and AB is the actual bitrate. And therefore, the difference bitrate accuracy Δacc between the proposed algorithm and the HM-14 is expressed as:

$$\Delta acc = acc_{proposed} - acc_{anchor} \quad (4)$$

As shown in Table I, the proposed algorithm can achieve up to 0.01% and 0.07% accuracy gain for both Class A and Class B on the top of HM-14.0, respectively. Furthermore, the tile level rate control for HEVC on multi-core platform can achieve very negligible bitrate accuracy loss about 0.07% on average.

Table 1. Percentage error in the actual bitrate

Sequences	TB (kbps)	HM14.0 (kbps)	Proposed (kbps)	Accuracy (%)		Δacc (%)
				HM14.0	Proposed	
Traffic	3000	3002.55	3002.26	99.92	99.92	0.01
PeopleOnStreet	3000	3004.24	3016.24	99.86	99.46	-0.40
NebutaFestival	3000	3004.56	3011.52	99.85	99.62	-0.23
Kimono	3000	3004.22	3003.18	99.86	99.89	0.03
ParkScene	3000	3004.45	3005.46	99.85	99.82	-0.03
Cactus	3000	3002.84	3001.86	99.91	99.94	0.03
BasketballDrive	3000	3003.01	3000.92	99.90	99.97	0.07
Average				99.88	99.80	-0.07

4. Conclusion

In this paper, the tile level rate control algorithm for multicore platform of HEVC is proposed. In the proposed algorithm, the allocation bits for each tile is derived by considering the predetermined weight from the picture level rate control. According to the performance evaluation results, the proposed rate control on tile level shows about 0.07% bit accuracy loss compared to HM-14.0.

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