# 인버터 모터 드라이브 시스템을 위한 새로운 1200V High Side Driver

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# Advanced 1200V High Side Driver for Inverter Motor Drive System

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## ABSTRACT

New inverter motor drive systems consume 30%~50% less energy compared to existing motor drive systems. For inverter motor drive systems, the development of a 1200V high side driver is critical. This paper presents an advanced 1200V high side driver with low power consumption and high ruggedness. This solution implements a high voltage level shifter which consumes low power by adding a clamped VGS LDMOS driver to the conventional short pulse generator. Moreover, this paper proposes a highly rugged 1200V LDMOS which improves SOA by limiting the hole current. This paper could be applied to smart power modules used for HVAC (heating, ventilation, and air-conditioning) and industrial inverters. Consequently, this paper will provide design engineers with an understanding of how they can make a significant contribution to worldwide energy savings.

## 1. INTRODUCTION

The depletion of natural resources and environmental problems caused by dramatically increasing energy consumption worldwide has of course emerged as a critical issue facing modern society. Electric motors alone consume about 41% of all of the world's electricity and most are used in industrial automation[1]. The inverter motor drive system saves upon electric consumption by 30~50% compared to existing motor drive systems, but they only make up less than 10% of all motor drive systems implemented worldwide. Thus, the necessity to use inverter motor drive systems is heightened to increase energy savings and the efficient use of energy. In addition, the demand for inverter motor drive systems is on the rise as the result of governmental regulations governing energy savings[2]. Inverter motor drive systems require high ruggedness of 1200V high side drivers because operating conditions are severe due to switching noise[3]. Therefore, the development of a 1200V high side driver is critical.

## 2. ADVANCED 1200V HIGH SIDE DRIVER

### 1.1 Challenges of the 1200V high side driver

There are important challenges in working with a 1200V high side driver. Firstly, it requires low power consumption of a high voltage level shifter. Secondly, it needs to prevent degradation of ruggedness of a 1200V lateral double diffused metal oxide semiconductor (LDMOS). To overcome these challenges, this paper presents an advanced 1200V high side driver which implements a proposed clamped VGS LDMOS driver and a high rugged 1200V LDMOS.

#### 1.1.1 Power consumption of high voltage level shifter

The high side driver contains a low side for transferring input control signals and a high side for driving the high side driver connected power switch devices, such as an insulated gate bipolar transistors (IGBTs). The high side is connected to the low side via a high voltage level shifter.

Because the high voltage (up to 1200V) rail is connected to the high voltage level shifter directly, it consumes a lot of power. Reducing the power consumption of the high voltage level shifter to drive the high side power switch device efficiently is one of the most important parts of the high side driver. For this reason, the high side driver definitely needs a short pulse generator (SPG) which reduces power consumption by driving the LDMOS of high voltage level shifter as a short pulse width[4]. We can write the average amount of current of the high voltage level shifter as:

$$I_{avg} = I_{peak} \times PW \times f_{sw} \times 2 \quad (1)$$

where $I_{peak}$ is the peak amount of current of the high voltage level shifter which increases along with the increase of the power supply (VDD), because as the value of VDD increases, the gate-source voltage (VGS) of LDMOS increases causing the drain current to increase. $PW$ and $f_{SW}$ indicate the pulse width of the output signal of the short pulse generator and the switching frequency of the input control signal, respectively. The average power dissipated by the high voltage level shifter is

$$P_{avg} = VB \times I_{avg} \quad (2)$$

Where, $VB$ is the voltage level of the high side floating supply which has up to 1200V. As we can see (1) and (2), the power consumption of the high voltage level shifter increases along with the increase of VB and VDD.

#### 1.1.2 Ruggedness of high voltage LDMOS

High voltage LDMOS ruggedness can be represented as safe operating area (SOA). The term SOA is used to describe the region in the ID-VDS plane through which the device can switch without suffering damage. The boundary of the SOA is under the control of the device designer. In all n-channel LDMOS, there is a parasitic npn transistor that can turn on under certain conditions. This can happen when a sufficient base-emitter voltage drops across the body and source junction. The forward bias is due to a hole current, where the holes are supplied by the carrier generation mechanisms. As the value of VB and VDD increase, the hole current increases causing the parasitic npn transistor turn on, arises an electrical snapback I-V phenomenon and the high voltage LDMOS is destroyed. It is called the electrical SOA[5].

### 2.1 Development of Advanced 1200V high side driver

The advanced 1200V high side driver is composed of a clamped VGS LDMOS driver which reduces the power consumption of the high voltage level shifter and a high rugged 1200V LDMOS which improves SOA by limiting the hole current.

### 2.1.1 Proposed clamped VGS LDMOS driver (CVLD)

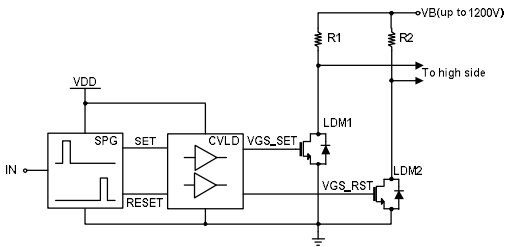


Fig. 1 Proposed clamped VGS LDMOS driver

Fig. 1 shows the proposed clamped VGS LDMOS driver (CVLD). This circuit is composed of a temperature compensated zener clamp circuit (TCZC) and an input clamped NMOS buffer. This circuit sets the limit for the VGS value of the LDMOS at a specific voltage level to reduce the power consumption of the high voltage level shifter. Moreover, the proposed circuit does not consume quiescent dissipation in quiescent condition. Where, VGS_SET and VGS_RST are the gate-source voltage of SET LDMOS and RESET LDMOS, respectively.

The VGS has constant and lower value than the power supply voltage using the CVLD. Furthermore, the VGS is specially designed to minimize temperature effects using the temperature coefficient. The TCZC is composed of a zener diode and a threshold voltage generation circuit. The zener diode will increase with increasing temperature. It has the proportional to absolute temperature (PTAT) voltage. On the other hand, the threshold voltage of NMOS will decrease with increasing temperature. It has the complementary to absolute temperature (CTAT) voltage. The sum of the zener voltage and the threshold voltage of NMOS will be able to achieve temperature compensation. Thus, the TCZC circuit is capable of compensating temperature variation.

In summary, the proposed clamped VGS LDMOS driver generates the supply insensitive and temperature independent VGS of the LDMOS which has lower value than the power supply. This constant and low VGS reduces the average current of the high voltage level shifter as the drain current of the LDMOS decreases. As a result, the power consumption of the 1200V high side driver has greatly decreased. In addition, it does not increase the power consumption along with the increase of the power supply voltage. Furthermore, the low VGS brings another great advantage, and that is, it is capable of preventing a degradation of the LDMOS ruggedness when VGS has high value.

### 2.1.2 Proposed high rugged 1200V LDMOS

As mentioned above, the electrical snapback phenomenon occurs due to increasing of the hole current by high VB and VDD. Therefore, this paper proposes the high rugged 1200V LDMOS which improved SOA by limiting the hole current. As reducing N+ source area of conventional LDMOS, it has decreased the current density per unit area. Consequently, it makes a dent in the amount of hole current, and it could also greatly improve the SOA of the 1200V LDMOS.

### 3.1 Simulation and measurement results

Fig. 2 shows the simulation results of the VGS value when VDD is 15V. As we can see from the figure, the VGS value of the conventional circuit is equal to VDD because it is fixed at the VDD by push-pull buffer. In contrast, the VGS value of the proposed circuit is 6.85V by CVLD. It clearly shows the proposed circuit generates the low VGS of the LDMOS. Low VGS value of the LDMOS can reduce the power consumption and achieve a more rugged 1200V high side driver. As shown in Fig. 3, the measurement results in the 1200V of VB shows high side driver peak current. The average power consumption of a conventional circuit is 262mW. In contrast, the average power consumption of the proposed circuit is only 84mW. From these results, the proposed circuit is capable of reducing the power consumption significantly by 68% compared to the conventional circuit. It also obtains high ruggedness which normally operates at all temperature ranges and higher than 1200V of VB without destroying the device.

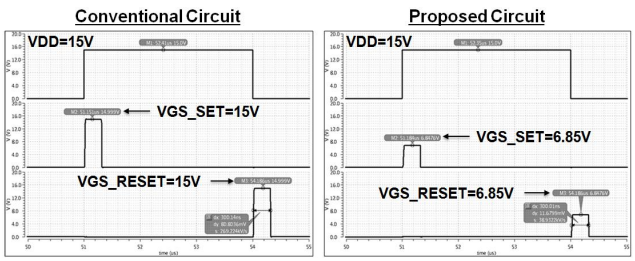


Fig. 2 VGS value of the LDMOS

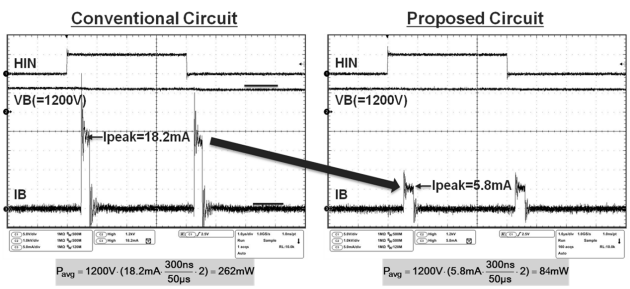


Fig. 3 High side driver peak current

## 3. CONCLUSION

In this paper, an advanced 1200V high side driver with a clamped VGS LDMOS driver and high rugged 1200V LDMOS is presented. The proposed clamped VGS LDMOS driver is able to significantly reduce high side driver power consumption. It does not increase along with the increase of the power supply. In addition, the low VGS value of LDMOS and the proposed high rugged 1200V LDMOS improve the SOA of 1200V LDMOS. The advanced 1200V high side driver could be applied to smart power module used for high power applications, such as HVAC and industrial inverters. It will be possible to meet the energy saving regulations of each country. Consequently, it will significantly contribute to worldwide energy savings.

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