고효율 서버용 전원 장치를 위한 하프-브리지 *LLC* 컨버터의 공진 커패시터 온-오프 제어

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Resonant Capacitor On/Off Control of Half-Bridge *LLC* Converter for High Efficiency Server Power Supply

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ABSTRACT

In this letter, a simple control method of the HB *LLC* converter with one additional switch and capacitor in the primary side is proposed for wide-input-voltage applications with the hold-up time conditions. At nominal input, since the proposed method enables the HB *LLC* converter to operate with large transformer magnetizing inductance, it can reduce the conduction and switch turn-off losses in the primary side, which makes a high efficiency. On the other hand, during the hold-up time, since the proposed method increases the resonant capacitance by turning on one additional switch, the HB *LLC* converter can obtain high voltage gain.

I. INTRODUCTION

The energy conversion efficiency in the server power supplies has become a very important issue in these days as the amount of electricity consumed in the data centers remarkably increases[1]. Especially, the necessity of the server power supplies with a high efficiency is emphasized on medium power (300-600W) supplies due to the server infrastructure for small companies. These server power supplies are composed of two-stage structure that has the boost power factor correction (PFC) stage and dc/dc stage. For this dc/dc stage, the half-bridge (HB) *LLC* converter has been widely used in medium power applications due to low component count, no transformer dc-offset current, and wide zero-voltage-switching (ZVS) range, which makes a high efficiency and high power density. Meanwhile, an important requirement in the server power systems is the hold-up time conditions[2]-[4] where its output voltage should be provided by the energy stored in the link capacitor to save the data during several milliseconds after AC line is lost. Therefore, the input voltage range in the dc/dc stage is wide. To satisfy the hold-up time conditions in the server power systems, the HB *LLC* converter should be designed to meet wide input voltage range, so small transformer magnetizing inductance is required to obtain high voltage gain. However, it causes large conduction and switch turn-off losses in the primary side at nominal input where a high efficiency is required.

Many papers have studied the hold-up time compensation method in order to achieve a high efficiency with large transformer magnetizing inductance at nominal input in the HB *LLC* converter, while high voltage gain is obtained during the hold-up time[2]-[4]. These approaches use auxiliary circuits or different control schemes. In [2], the converter makes higher voltage gain by increasing the transformer secondary turns during the hold-up time. However, it uses many additional semiconductor devices or transformer windings which cause the circuit complexity. In [3], the HB *LLC* converter with boost pulse-width-modulation (PWM) control method is proposed, and the HB *LLC* converter with asymmetric PWM control method is proposed in [4]. These methods can obtain high voltage gain due to their PWM control methods during the hold-up time. However, commonly, the transformer dc-offset current caused by their PWM control methods increases the transformer size. Moreover, they require additional PWM control methods which are complex.

In this letter, a simple control scheme of the HB *LLC* converter with one additional switch and small-sized multi-layer ceramic capacitor (MLCC) is proposed for wide-input-voltage applications with the hold-up time conditions. The HB *LLC* converter with the proposed control scheme has the following operations and advantages according to the input voltage: 1) At nominal input where one additional switch is turned off, the proposed method enables the HB *LLC* converter to operate near the resonant frequency with large transformer magnetizing inductance. Therefore, it can achieve a high efficiency due to small conduction and switch turn-off losses in the primary side. 2) During the hold-up time, since the proposed method increases the resonant capacitance by turning on one additional switch, the HB *LLC* converter can obtain high voltage gain.

II. DESCRIPTION OF THE PROPOSED CONTROL METHOD

A. Concept of Proposed Method

The voltage gain M of the HB *LLC* converter can be expressed as follows:

$$M = \frac{nV_O}{V_S} = \frac{1}{2\sqrt{\left\{1+\frac{1}{k}\left[1-\left(\frac{f_R}{f_S}\right)^2\right]\right\}^2 + \left[\frac{\pi^2 Q}{8n^2}\left(\frac{f_S}{f_R}-\frac{f_R}{f_S}\right)\right]^2}}, \quad (1)$$

where $k=L_m/L_R$, $Q=(L_R/C_R)^{0.5}/R_O$, $f_R=1/[2\pi(L_RC_R)^{0.5}]$, $n=N_P/N_S$, and f_S is the switching frequency. In the HB *LLC* converter, k factor mainly affects the slope of the voltage gain around the resonant frequency f_R, and its maximum voltage gain is affected by Q factor. Moreover, the HB *LLC* converter is generally designed to operate near f_R in order to obtain maximized efficiency at nominal input, i.e., $f_S \approx f_R$.

In wide-input-voltage applications with the PFC stage, there are two considerations in designing the resonant tank of the HB *LLC* converter: first, it is desirable that the HB *LLC* converter is designed with low/middle k factor to have small frequency variation at nominal input due to 120Hz input voltage ripple generated by the PFC stage. Secondly, the HB *LLC* converter should be designed with small transformer magnetizing inductance L_m to cover wide input voltage. If L_m is decreased under the same low/middle k factor conditions, the resonant inductance L_R is decreased by small L_m, and the resonant capacitance C_R is increased under fixed f_S, i.e., $f_S \approx f_R$ at nominal input. As a result, Q factor, i.e., $Q=(L_R/C_R)^{0.5}/R_O$, is considerably decreased, thus this design can meet required maximum voltage gain because of low Q factor. However, small L_m causes the HB *LLC* converter to have large conduction and switch turn-off losses in the primary side at nominal input. Therefore, to achieve a high efficiency at nominal input, the HB *LLC* converter should

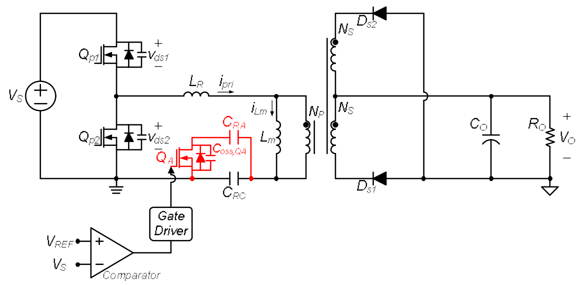
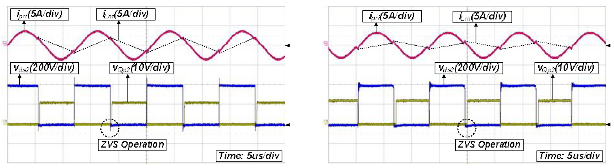


Fig 1 Proposed converter



(a) Conventional HB LLC converter (b) Proposed converter

Fig 2 Operational key waveforms at nominal input

have large L_m. However, if the HB *LLC* converter is designed with large L_m under the same low/middle k factor conditions, L_R is relatively increased by large L_m compared with the previous case, and C_R is decreased under fixed f_S, i.e., $f_S \approx f_R$ at nominal input. As a result, Q factor is relatively increased, thus this design cannot meet required maximum voltage gain. Meanwhile, in the proposed method, Q factor is decreased by increased C_R by turning on one additional switch during the hold-up time. Therefore, the voltage gain is increased despite large L_m.

B. Operational Principles

In the proposed converter as shown in Fig. 1, one additional switch and capacitor are employed to increase the voltage gain during the hold-up time maintaining large L_m. C_R is changed by turning on or off one additional switch Q_A only according to the input voltage.

At nominal input, Q_A is turned off, and the voltage across the output capacitance $C_{oss,QA}$ of Q_A is almost the voltage across C_{RC} due to small $C_{oss,QA}$. As a result, the body diode of Q_A is blocked, and $C_{oss,QA}$ is connected in series with one additional capacitor C_{RA}. Since $C_{oss,QA}$ is small enough compared with C_{RA}, the resonant capacitance C_R almost becomes C_{RC}, i.e., $C_R = C_{RC} + C_{RA} // C_{oss,QA}$. The added circuit for the hold-up time conditions does not affect the operation of the HB *LLC* converter at nominal input where a high efficiency is required. During the hold-up time, Q_A is turned on. C_{RC} is connected in parallel with C_{RA}, and C_R almost becomes $C_{RC}+C_{RA}$. It means that C_R is increased during the hold-up time compared with that at nominal input, thus low Q factor can be obtained, which results in high voltage gain.

III. Experimental Results

The proposed converter has the following specifications for the server power systems: nominal input voltage=385V, output voltage=56V, and rated power=350W. The components list is presented in Table I.

Fig. 2(a) and 2(b) show the operational key waveforms of the conventional and proposed converters in full load condition at nominal input, respectively. From these figures, it is noted that the slope of i_{Lm} in the proposed converter is more gradual than that in the conventional converter due to large L_m satisfying the ZVS operation, which reduces the conduction and switch turn-off losses in the primary side. Fig. 3 shows the operational key

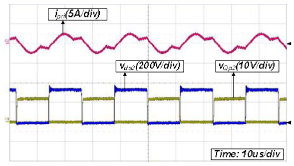


Fig 3 during hold-up time

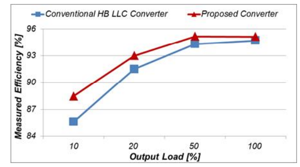


Fig 4 Measured efficiency

Table I Design Parameters

Components list	Conventional HB *LLC* converter	Proposed converter
Transformer	Core: PQ2625 (A_e=118mm^2)	
	L_m=322 74µH	L_m=642 50µH
	N_P:N_S:N_S=24:7:7	
Resonant capacitance	C_{RC}=66nF	C_{RC}=44nF, C_{RA}=78nF
Resonant inductance	L_R=53 79µH	L_R=76 87µH
Secondary diodes	STPS30150 (150V/30A, V_F=0 75V)	
Additional switch	–	SIHP25N40D

waveforms of the proposed converter in full load condition during the hold-up time. From this figure, it is noted that the resonant frequency f_R during the hold-up time is decreased more than that at nominal input due to increased C_R, and f_S is reduced below f_R to obtain high voltage gain. Fig. 4 shows the measured efficiency of the conventional HB *LLC* and proposed converters at nominal input. The efficiency of the proposed converter is improved over the entire load conditions, especially under light load conditions due to small conduction and switch turn-off losses in the primary side, resulting from large L_m.

IV. Conclusion

In this letter, a HB *LLC* converter with a simple control scheme using one additional switch and small-sized MLCC is proposed. The resonant capacitance is changed by turning on or off one additional switch only according to the input voltage. During the hold-up time, since the proposed method increases the resonant capacitance by turning on one additional switch, the HB *LLC* converter can obtain high voltage gain. Due to this increased voltage gain, the proposed converter is designed with large transformer magnetizing inductance at nominal input. At nominal input, one additional switch is turned off, and the resonant capacitance is decreased, which enables the proposed converter to operate near the resonant frequency. Therefore, it can achieve a high efficiency due to small conduction and switch turn-off losses in the primary side.

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