Neutral Point Balancing Algorithm for Multi-level Converter under Unbalanced Operating Conditions

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Abstract

This paper presents a neutral point deviation compensating control algorithm applied to a 3-level NPC converter. The neutral point deviation is analyzed with a focus on the current flowing out of or into the neutral point of the dc link. Based on the zero sequence components of the reference voltages, this paper analyzes the neutral point deviation and balancing control for 3-level NPC converter. An analytical method is proposed to calculate the injected zero sequence voltage for NP balancing based on average neutral current. This paper also proposes a control scheme compensating for the neutral point deviation under generalized unbalanced grid operating conditions. The positive and negative sequence components of the pole voltages and ac input currents are employed to accurately explain the behavior of 3-level NPC converter. Simulation and experimental results for a test set up of 30kW are shown to verify the validity of the proposed algorithm.

1. Introduction

Multi-level converters are widely used in high-power applications such as motor drives, utility applications, and, most recently, in wind generation systems. Extensive research has been carried out on multilevel topologies, modulation, and control strategies [1]. Multilevel converters can provide more than two voltage levels at the output. As a result, the voltage and current waveforms generated have lower Total Harmonic Distortion (THD). Consequently, high voltages can be handled on both the dc and ac sides of the converter [2].

The multilevel converter topology that is most extensively applied at present is the Neutral-Point-Clamped (NPC) converter, which is a 3-level NPC Voltage Source Converter (VSC) in Fig. 1. One of the essential problems of the 3-level NPC converters is that how to keep the voltage of dc-link capacitors balanced, in other words, keep the Neutral-Point (NP) potential stable and suppress the ripple. If the NP potential is not controlled effectively, the output voltage of the converter would deviate from the reference value; moreover, the devices and equipment might be damaged [3]. In practical operations of 3-level NPC VSC, the NP potential variation, in other words, the unbalanced dc link voltages often lead to a frequent trip of converters due to the over-voltage of either upper dc link capacitor or lower dc link capacitor. The control strategies of NP potential that have appeared in the literatures can be grouped according to the Pulse Width Modulation (PWM) algorithm utilized. If Space Vector PWM (SVPWM) is used, the voltage vectors can be classified into four categories by their magnitude: zero, small, middle, and large vectors. Then, the relationship between NP potential and each switching state vector can be analyzed. It is known that the zero vectors and large vectors have no effect on NP potential, but the middle vectors and small vectors can have an influence on it. It is noticed that there are two switching states (positive and negative) that have reverse action (charging or discharging) on NP potential for one small vector. Therefore, the main task is to adjust the dwell time between the duplicate switching states of small vectors [4]–[9]. In many solutions of the SVPWM strategies for the 3-level NPC converter, one or two switching sequences are strictly assigned to specific subsectors [10], [11]. The control strategies of the dc-link voltage balance are based on the change of switching sequences depending on the unbalanced dc-link voltage. When Carrier-Based PWM (CBPWM) is used, the control of the NP potential can be considered as the problem of identifying the zero sequence voltage. The zero sequence voltage added to the reference voltages does not change the output line voltages, but influences the switching states and of course the NP potential. The NP potential variation caused by the injected zero sequence voltage has been studied, and some algorithms to keep the NP potential balancing by injecting the appropriate zero sequence voltage were presented.

Among many possible causes of NP deviation in 3-level NPC converters, unbalanced grid supply can generate NP deviation of significant level. The impact of unbalanced grid input on the NP deviation and suitable compensating control strategies have been paid less attention considering its importance in a practical operation. Also, none of previous works have deeply analyzed the relationship between unbalanced grid condition and NP deviation under the wide range of unbalanced condition within a 3-level NPC converter.

This paper proposes a CB-PWM strategy for a 3-level NPC converter with a zero sequence voltage injection. In this paper, the variation of the neutral point potential is analyzed on the basis of an average current flowing out of or into the neutral point. It is shown that the zero sequence voltage of the NPC-VSI output has an important influence upon the neutral potential variation. The principle of the neutral point potential control by adding a suitable zero sequence voltage is also described. Moreover, this paper proposes NP deviation control scheme for the 3-level NPC converter under generalized unbalanced grid operating conditions. The positive and negative sequence components of the pole voltages and ac input currents are employed to accurately explain the behavior of 3-level NPC converter and its impact on NP deviation. The proposed CB-PWM compensating strategy is verified by the real-time simulator of Typhoon HILS. This test equipment provides a real time operating environment of DSP (TI TMS320F28335) so that the effective verification of the proposed compensating algorithm is made possible, without performing a time-consuming real hardware experiment.

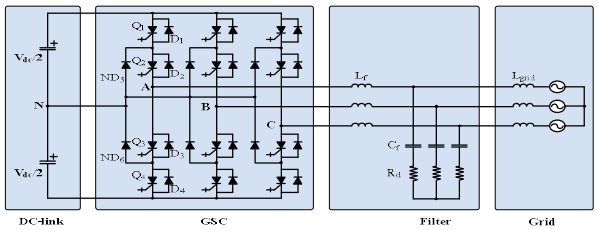


Fig. 1. 3-level NPC voltage source converter

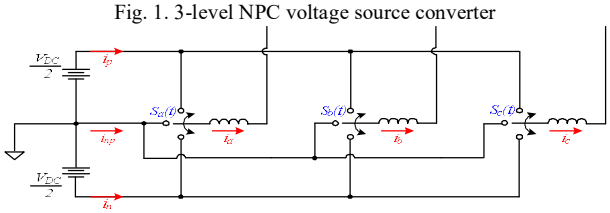


Fig. 2. Simplified converter using SPTT (Single-pole-Triple-Throw)

2. Relationship between Neutral Point Deviation and Average Neutral Current

Figure 2 describes simplified 3-level NPC converter using Single-Pole-Triple-Throw switches. Average neutral current and zero sequence voltage components in dc-link are expressed as following. In general, Neutral current can be described by each phase current and switching function as in (1)-(2). Converter output voltage can be represented by switching function as in (3). Average neutral current can be explained by fundamental voltage of switching function and its corresponding current as in (4).

$$V_{ss} = (S_a, S_b, S_c), S_x = [-1,0,1] \,\&\, x = a,b,c \tag{1}$$

$$\begin{aligned} i_{np}(t) &= [1-|S_a|]\cdot i_a + [1-|S_b|]\cdot i_b + [1-|S_c|]\cdot i_c \\ &= -(|S_a|\cdot i_a + |S_b|\cdot i_b + |S_c|\cdot i_c) \end{aligned} \tag{2}$$

$$V_{x\_pole} = S_x(t) \times \frac{V_{dc}}{2}, x = a,b,c \tag{3}$$

$$v_0 = -\left\{ \frac{\frac{2}{V_{dc}}\cdot i_{NP} + \mathrm{sgn}(v_a)\cdot v_{a\_fund}\cdot i_a + \mathrm{sgn}(v_b)\cdot v_{b\_fund}\cdot i_b + \mathrm{sgn}(v_c)\cdot v_{c\_fund}\cdot i_c}{\mathrm{sgn}(v_a)\cdot i_a + \mathrm{sgn}(v_b)\cdot i_b + \mathrm{sgn}(v_c)\cdot i_c} \right\} \tag{4}$$

3. Analysis of Neutral Point Deviation based on Generalized Unbalanced 3-phase Grid Condition

Under unbalanced grid condition, converter output voltage can be effectively analyzed by using both positive and negative sequence components of converter output voltages and currents in grid-side converter and input filter. This paper proposes control scheme to actively compensate for the neutral point deviation of 3-level NPC converter by controlling PWM reference voltage. For example, balanced neutral point voltage implies that the negative and zero sequence reference voltage must be zero. Fundamental voltage of PWM and output current can be represented by using positive, negative, and zero sequence voltage as in (5). Neutral current can be explained the using fundamental voltage of switching function and current based on symmetrical components as in (6). As a result, the average neutral current consists of dc offset and harmonics term under unbalanced gird condition. DC offset term occurs the neutral point deviation in 3-level NPC converter. This paper proposes control scheme can be obtained from (7).

$$v_{x\_fund} = v_{xp} + v_{xn} + v_o,\ i_x = i_{xp} + i_{xn}, x = a,b,c \tag{5}$$

$$i_{np}(t) = -\frac{2}{V_{dc}}\left\{ \begin{aligned} &\mathrm{sgn}(v_{a\_fund})\cdot(v_{ap} + v_{an} + v_o)\cdot(i_{ap} + i_{an}) + \mathrm{sgn}(v_{b\_fund})\cdot(v_{bp} + v_{bn} + v_o)\cdot(i_{bp} + i_{bn}) \\ &+ \mathrm{sgn}(v_{c\_fund})\cdot(v_{cp} + v_{cn} + v_o)\cdot(i_{cp} + i_{cn}) \end{aligned} \right\} \tag{6}$$

$$i_{np}(t) = -\frac{1}{V_{dc}}\left\{ (X+Z) + \sqrt{N^2+L^2}\cos(\omega t - \alpha) + \sqrt{Y^2+(X-Z)^2}\cos(2\omega t - \rho) + \sqrt{M^2+K^2}\cos(3\omega t - \beta) \right\} \tag{7}$$

$$\alpha = \tan^{-1}\left(\frac{N}{L}\right), \beta = \tan^{-1}\left(\frac{Y}{X-Z}\right), \text{and } \rho = \tan^{-1}\left(\frac{M}{K}\right)$$

4. Experimental Results using HILS

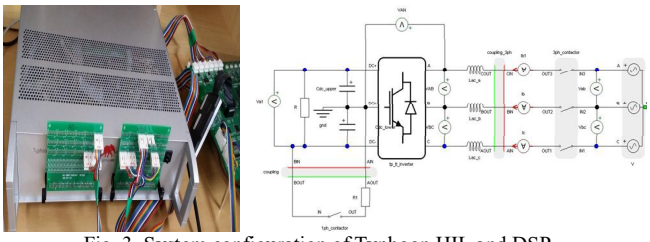


Fig. 3. System configuration of Typhoon HIL and DSP

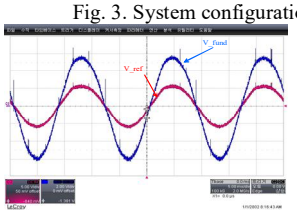


Fig. 4. Waveforms of reference voltage and modulation signal

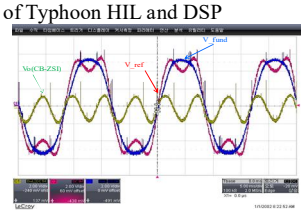
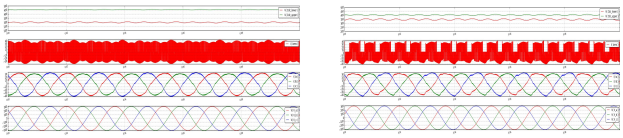


Fig. 5. Waveforms of reference voltage, modulation signal and calculated zero sequence voltage



(a) (b)

Fig. 6. Waveforms of dc-link voltage and grid current using Typhoon ((a) without compensating algorithm, (b) with compensating algorithm)

Figure 3 shows schematic diagram for hardware-in-the-loop simulator (HILS). Figure 4 describes reference voltage of current regulator output and modulation signal for PWM operation. Figure 5 shows fundamental voltage with calculated zero sequence voltage. Figure 6 present the real time simulation result; one is without compensating algorithm and the other is with compensating algorithm. These waveforms include dc-link voltage, neutral current, grid current, and voltage.

5. Conclusion

This paper presents the analysis of the neutral point potential variation of 3-level NPC converter. An analysis is carried out based on the average current flowing at the neutral point of the dc link. A control scheme to keep the dc-link voltages balanced is also proposed. The potential variation can be eliminated or reduced by controlling the zero sequence voltage. In this paper, control scheme for compensating a neutral point deviation under unbalanced grid conditions is also investigated. This control scheme can be effectively analyzed by using both positive and negative sequence components of converter output voltages and ac input currents. Typhoon HILS test environment confirms that the proposed control scheme makes it possible to reduce the neutral point potential variation.

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