대기전력 최소화를 위한 교류전압 입력에 따른 저전압 구동회로 설계

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Standby Power Reduction Technique due to the Minimization of voltage difference between input and output in AC 60㎐

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Abstract - Recently, standby power reduction techniques of AC/DC adaptor were developed, consuming power almost arrived to 300㎽ level. The standby power losses are composed of the input filter loss 11.8㎽, the control IC for AC/DC adaptor 18㎽, the switching loss 9.53㎽ and the feedback loss 123㎽. And there are the standby power reduction techniques. In this paper, in order to reduce the standby power of SMPS more, the loss due to a voltage difference between input and output is reduced by the control circuit which is composed of the low voltage driving circuit and voltage regulator. The low voltage driving circuit operates on the low voltage of input and off the high voltage. The low voltage driving IC was produced by the 1.0㎛, high voltage DMOS process.

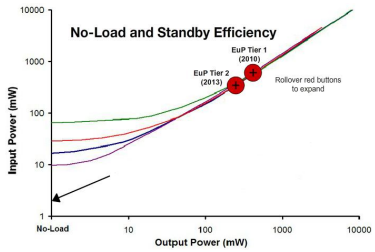
1. Introduction

International Energy Agency announced that the standby power of OECD member country is 10% level of power consumption per house. In the case of USA, the 5% of total electrical power consumption is the standby power and when changes money reaches to 1.3 billion dollar. Total standby power of Korea house is about 618MW and power that will be able to supply to 1.2 million house, and correspond to one thermal power generation.

And each country consider many kind method to reduce the standby power, energy star program in USA and EuP Tier program in EU recommend the standby power level as 50㎽ of AC/DC adaptor. The standby power of fly-back converter with under 5W is reached to 3㎽ by PI. The standby power of under 5㎽ is regarded as 0W in IEC 62301

Recently, standby power reduction techniques of AC/DC adaptor were developed, consuming power almost arrived to 300㎽ level. The standby power losses are composed of the input filter loss 11.8㎽, the control IC for AC/DC adaptor 18㎽, the switching loss 9.53㎽ and the feedback loss 123㎽[1].

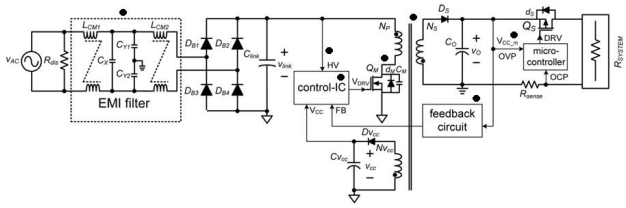
Fig 1 shows the relationship of input power and output power, the smaller output and input power, the lower efficiency. It is necessary to upgrade the efficiency of fly-back converter on the light load. This is how to reduce the standby power of the fly-back converter of which consumer electronics are composed.



<Fig 1> No-load and standby power efficiency

There is a various standby power reduction method that is (1) Reduction of power consumption in startup resistor [4,5], (2) Reduction of switching frequency[3,7], (3) Reduction of output voltage disconnection, (4) Output voltage drop, (5) Use of a low-power auxiliary power supply [3]. Other proposals also include using burst mode [3,6,7] to keep the dc link voltage steady, the design of low-loss semiconductor integrated circuits [8-10] and adoption of control mechanism [7] and algorithm for standby power reduction.

Fig 2 show typical SMPS circuit and the power consumption of EMI filter is 11.8㎽, control IC 18㎽, switching loss 9.53㎽ and feedback loss 123㎽ at each part on the standby mode. Total standby power of SMPS is 165㎽.



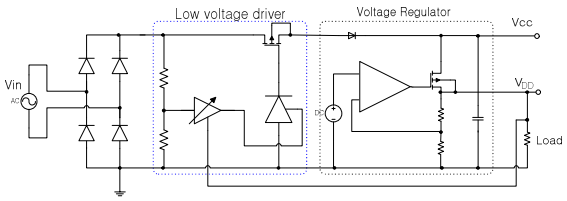
<Fig 2> Standby power loss in each part of SMPS

In this paper, in order to reduce the standby power of SMPS more, the loss due to a voltage difference between input and output is reduced by the control circuit which is composed of the low voltage driving circuit and voltage regulator.

2. Proposed standby power reduction circuit

2.1 Proposed circuit for minimization of standby power

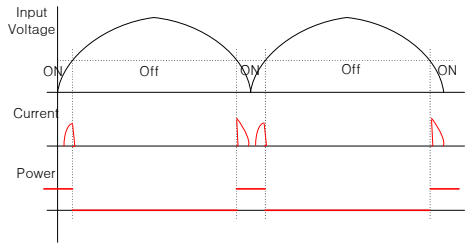
To reduce the standby power of SMPS more, the loss due to a voltage difference between input and output is reduced by the control circuit in Fig 3. Proposed circuit is composed of the low voltage driving circuit and voltage regulator. The low voltage driving circuit operates on the low voltage of input and off on the high voltage input. Circuit operation principle is as in the following.



<Fig 3> Proposed circuit to reduce the standby power

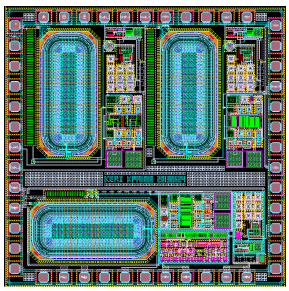
Comparator of low voltage driver feed voltage of resistor divider in Fig 3 and set value, if feeding voltage > set value, output 2.5V high voltage on the comparator and shunt regulator is commuted, power MOSFET is turned off. If feeding voltage < set value, output 0V voltage on the comparator and shunt regulator is turned off, power MOSFET is turned on. Thus proposed circuit supply power in the case of feeding voltage > set value as waveform of Fig 4. Fig 4 is

shown that the waveform of input voltage, current and power. So the loss due to voltage difference between input and output is reduced and the standby power is reduced.



<Fig 4> Input voltage, current and power waveform of proposed circuit

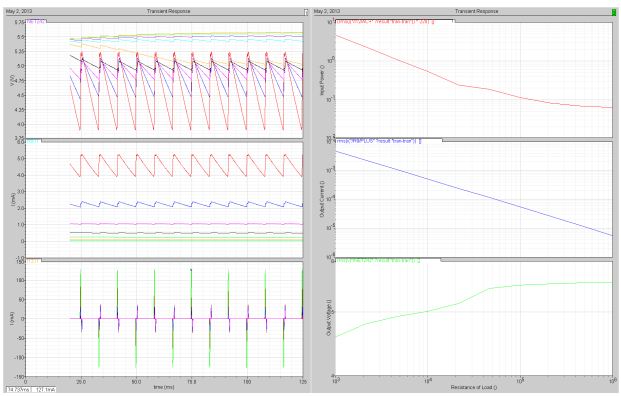
The low voltage driving IC was produced by the 1.0㎛, high voltage DMOS process. Fig 5 is shown that three core chips are in a die.



<Fig 5> Manufactured chip layout of proposed circuit

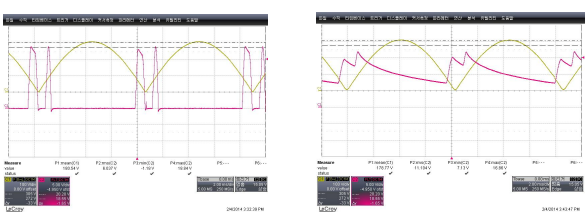
2.2 Simulation and experimental results

Fig 6 shows the result that are output voltage, output current and input current depended upon time on the left side of figures, input power, output current and output voltage depended upon resistance of load on the right side. The bottom on the left side of Fig 6 similar with the current waveform of Fig 4. It is confirmed that the proposed circuit is operated well.



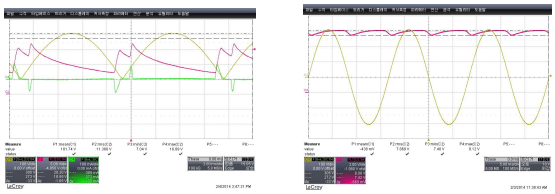
<Fig 6> Electrical characteristics of proposed circuit by simulation

Fig 7 show the input voltage and current waveform on the left side output voltage and input voltage at load 5.6kΩ.



<Fig 7> Waveform @ load 5.6kΩ, V_{out}=7.7V

Fig 8 shows the waveform of input voltage, output voltage and current at load 5.6kΩ and MLCC 9.4㎌.



<Fig 8> Waveform @ load 5.6kΩ, V_{out}=7.7V

It was confirmed that the proposed circuit operate well by the testing of manufacturing chip.

3. Conclusion

In this paper, in order to reduce the standby power of SMPS more, the loss due to a voltage difference between input and output is reduced by the control circuit which is composed of the low voltage driving circuit and voltage regulator. The low voltage driving circuit operates on the low voltage of input and off the high voltage. The low voltage driving IC was produced by the 1.0㎛, high voltage DMOS process. Proposed standby power reduction circuit with low voltage difference between input and output was confirmed by testing chip.

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