CMOS Inverter Design based on Double Gate Ultra-Thin Body MOSFETs

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Ultra-thin body transistor is one of the emerging devices since it control leakage current flows through substrate. In addition, it can be operated by double gates, thus, its on/off current ratio is higher than conventional counterpart. In this paper, we design and investigate a CMOS inverter based on ultra-thin body MOSFETs to estimate its performance in real application. NEGF (non-equilibrium Green's function) method is used to obatain relationship between drain current and voltage. DC transfer is extracted from the relationship, and FO4 (fanout-of-4) propagation delay is reported as 5.1 ps estimated by a simple model.

I. INTRODUCTION

For sub-20 nm region, conventional semiconductor devices have been faced with several limitations. In this dimension, controlling leakage current gets more difficult. Due to its structural and electronic properties, ultra-thin body (UTB) devices are considered as one of the most promising candidates to suppress leakages flowing through substrate. In UTB devices, potential barrier between source and drain is strongly coupled to gate than the drain since they are made by quantum confinement along one direction (their height direction especially). Therefore, controlling the leakage currents can well be done [1]. In addition, UTB devices have higher on/off current ratio than conventional counterpart, which are not confined.

Considering those properties, UTB devices are favorable for CMOS logic circuits. In this paper, we design and investigate a CMOS inverter (inverter shortly) based on UTB MOSFETs to estimate its performance in real application. As channel and oxide materials, Si and SiO_2 are taken into account, respectively. UTB transistors can be operated with single or double gates. In view of device performance (related to on current), double gate UTB (DG-UTB) transistors are better. We, thus, consider DG-UTB MOSFET here. NEGF formalism is used to obtain relationship between drain current and voltage, assuming that electron transport is ballistic. It is implemented by software in EDISON [2]. From the relationship, input/output characteristic of inverter is extracted. Propagation delays are calculated by a simple model that we will discuss later.

II. METHODOLOGY

A. DC Transfer (Input/Output Characteristic)

Fig. 1 illustrates schematic of an inverter with load capacitor. An inverter consists of p- and n-type MOSFETs (pMOS and nMOS in short). V_{in} and V_{out} denote input and output voltage of inverter, respectively. The values of them are between V_{ss} and V_{dd}. V_{dd} (V_{ss}) is supply voltage

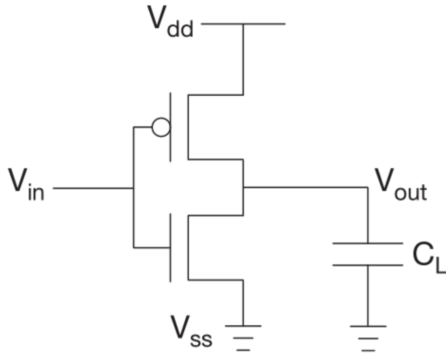

Fig. 16. Schematic of an inverter with load capacitor.

(ground) and implies logical '1' ('0'). C_L is capacitance of load capacitor. When V_{in} is V_{ss} (V_{dd}), pMOS (nMOS) is turned on and nMOS (pMOS) is turned off. Then, current flows through pMOS (nMOS) and load capacitor is charged (discharged). Consequently, V_{out} becomes V_{dd} (V_{ss}).

The output voltage of inverter is determined by the amount of charged in load capacitor. Therefore, to extract DC transfer of inverter, for each gate voltage, it is essential to know relationship between drain current (I_d) and voltage (V_d) of each MOSFET. We obtained the relationships by using UTB MOSFET quantum transport simulator in EDISON. From the results, we first make pMOS to be 2.14 times wider than nMOS such that charging and discharging current are the same. This is accomplished by multiplying 2.14 by the obtained drain current values of pMOS. After that, we pick two I_d-V_d curves; one for pMOS and the other for nMOS, which are correspond for the same V_{in} that can be written by

$$V_{in} = \begin{cases} V_{gp} + V_{dd} & \text{for pMOS} \\ V_{gn} + V_{ss} & \text{for nMOS} \end{cases} \quad (1)$$

where V_{gp} and V_{gn} are gate voltages of pMOS and nMOS, respectively. By finding an intersection point of the two picked curves, V_{out} is obtained. DC transfer can be plotted by performing above for all input voltages that we consider. The details of the extraction is in [3].

B. Propagation Delay

When V_{in} falls, rising propagation delay (t_{pdr}) is defined as the time taken to charge load capacitor from 0 to $V_{dd}/2$. Falling propagation delay (t_{pdf}) is defined similarly. Average propagation delay (t_{pd}), which is one of the most important information of logic circuit elements, is the average value of t_{pdr} and t_{pdf}. Numerically, for load capacitor, propagation delays can be obtained by solving differential equation

$$i(t) = C_L \frac{d}{dt} v(t) \quad (2)$$

where i(t) and v(t) are transient response of current and voltage, respectively. In quantum picture, transient responses can be obtained by solving time-dependent Schrödinger equation. However, its compuational cost is too expensive. Therefore, we use a simple delay model presented in [3]. The model estimates propagation delays with saturation current and supply voltage. From [3], t_{pdr} and t_{pdf} are written by

$$t_{pdr} = \alpha \frac{C_L V_{DD}}{I_{on,r}} \quad (3)$$

$$t_{pdf} = \alpha \frac{C_L V_{DD}}{I_{on,f}} \quad (4)$$

Parameter	Value
ε_{ox}	$3.9\varepsilon_0$
t_{ox}	1 nm
L	20 nm
W	Infinite (W >> L)

C'_{ox}	0.0345 F/m^2
C'_g	0.69 fF/μm

Table 14. Parameters for propagation delay estimation of UTB inverter.

where $I_{on,r}$ ($I_{on,f}$) indicates saturation current when V_{out} is rising (falling). In general, α is 0.5 assuming that V_{in} is ramp function. In [3], α is given as 0.7, which is obtained by circuit simulation results. Here, 0.7 is used for α.

To calculate t_{pdr} and t_{pdf} by using delay model given by (3) and (4), it is essential to determine saturation currents ($I_{on,r}$ and $I_{on,f}$), V_{dd}, and C_L. Saturation currents are obtained from relationship between drain current and voltage as we disscussed in II-A, , and we set V_{dd} to 0.7 V. Now, the key to estimate propagation delays is how to set C_L. In general, load capacitor consists of two components: next stage input capacitance (C_g) and output parasitic capacitance (C_p). The former is determined by calculating total gate capacitance of MOSFETs loaded by inverter, and the latter is diffusion capacitance of inverter. For the sake of simplicity, we neglect C_p here. C_g is given as

$$C_g = C'_{ox} \cdot L \cdot W \quad (5)$$

where C'_{ox} is oxide capacitance per unit area. L and W are the oxide length and width, respectively. We assume W>>L (valid in UTB devices), thus, we introduce new parameter $C'_g=C_g/W$ and use it hereafter instead of C_g. C'_{ox} is represented as ε_{ox}/t_{ox} where ε_{ox} is permittivity of oxide, and t_{ox} is oxide thickness. The parameters for propagation delay estimation are presented in Table I. Finally, C_L can be written as

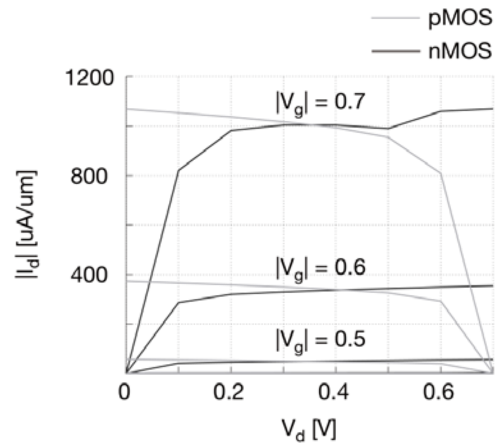

Fig. 2. I_d-V_d characteristics of pMOS and nMOS.

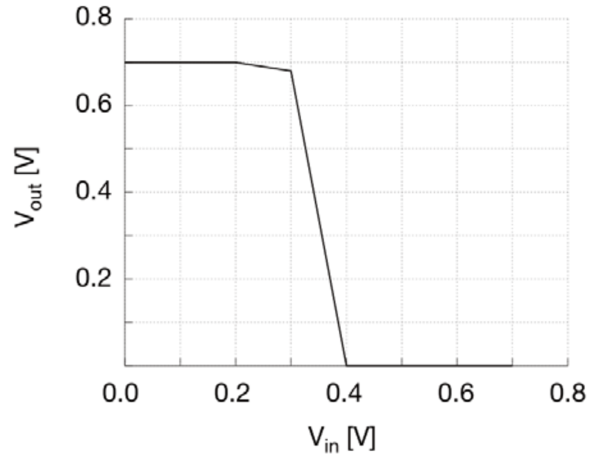

Fig. 3. DC transfer of inverter.

$$C_L = 2 \cdot C'_g \cdot N \quad (6)$$

where N is the number of MOSFETs loaded by inverter. The number 2 implies loaded MOSFETs also have double gates.

Load	N	Propagation delay (ps)		
		t_{pdr}	t_{pdf}	t_{pd}
Inverter	2	1.3	1.3	1.3
Two inverters	4	2.5	2.5	2.5
FO4	8	5.1	5.1	5.1

Table 2. Estimated propagation delays of DG-UTB

inverter with example loads.

III. RESULTS AND DISCUSSION

Fig. 2 shows I_d-V_d characteristics of pMOS and nMOS. As we discussed in II-A, magnitude of driving currents are equalized (see Fig. 2) by widening pMOS. DC transfer of our inverter is illustrated in Fig. 3. Logic threshold, which is defined as V_{in}=V_{out}, is about 0.35 V that is half of V_{dd}. Therefore, the inverter operates as a common inverter. Table II reports calculated propagation delays of the inverter. Propagation delay of FO4 (fanout-of-4 inverter) often represents refence delay of digital circuit. From [3], it ranges from 16 to 25 ps in 65 nm process (supply voltage is above 1.0 V in this process). For inverter in this paper, FO4 delay is about 5.1 ps with coherent transport and 0.7 V of supply voltage. Lower power consumption can be expected if the delay is comparable to that in 65 nm process since the supply voltage is much lower in the process (20 nm) considered in this paper.

IV. CONCLUSION

In this paper, we have designed DG-UTB based inverter. DC transfer is obtained from I_d-V_d characteristics obtained from quantum transport simulation. Propagation delay is calculated by using a simple model, and we can expect lower power consumption from the estimated delay.

A great deal of work are left to attain more exact results. Scattering effects have to be taken into account in NEGF. Solving time-dependent NEGF can supply transient response in nanoscaled dimension.

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