SRP 를 기반으로 하는 8K 프로그래머블 멀티미디어 플랫폼

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8K Programmable Multimedia Platform based on SRP

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Abstract

In this paper, we propose a world's first programmable video processing platform for video quality enhancement of 8K (7680x4320) UHD (Ultra High Definition) TV at 60 frames per second. To support huge computation and memory bandwidth of video quality enhancement for 8K resolution, the proposed platform has unique features like symmetric multi-cluster architecture for data partitioning, ring data-path between clusters to support data pipelining, on-the-fly processing architecture to reduce DDR bandwidth, flexible hardware to accelerating common kernel in video enhancement algorithms. In addition to those features, general programmability of SRP (Samsung reconfigurable processor) as main core of the proposed platform makes it possible to upgrade continuously video enhancement algorithm even after the platform is fixed. This ability is very important because algorithms for 8K DTV is under development. The proposed sub-system has been embedded into SoC (System on Chip) and new 8K UHD TV using the programmable SoC is expected at CES2015 for the first time in the world.

1. INTRODUCTION

4K (3840x2160) UHD[1] system has been studied and developed as broadcast standard for the next generation digital TV. NHK Science & Technology Research Laboratories proposed the 4K UHD video format, and it is defined and approved by the International Telecommunication Union (ITU).

In addition to 4K system, 8K[2] UHD TV system has been developed recently. 8K UHD TV has sixteen times as many pixels as current FHD (1920x1080) TV.

UHD TV including 4K and 8K doesn't have the mature video enhancement algorithm because it is not fixed yet and is being improved continuously. Unlike video decoder such as H.264 and HEVC which has been standardized, the video enhancement algorithms are upgraded on an ongoing basis.

Demand for the embedded system is increasing in the area such as the video post processing which can be applied to multiple algorithms by program update when compared to the H/W that cannot be changed once created. The use of embedded system is essential in order to respond to the algorithm change of video enhancement of image quality in high-definition TV sets in real time.

In this paper, we propose a world's first 8K real time video post processing platform. A system for post video processing is proposed to facilitate DSP and H/W accelerator. The platform gets the hybrid architecture – SRP cores with H/W accelerators – in order to maximize the SRP operation.

The remainder of this paper organized as follows. Section II gives a platform architecture including internal sub modules. In section III, the performance of the proposed sub-system is described. The applications by the platform are presented in section IV. The conclusion is followed in section V.

2. PLATFORM ARCHITECTURE

A. Problem Definition

8K UHD TV has 16 times as many pixels as current FHD (1920x1080) TV. Considering the 12bit pixel of 8K resolution, the amount of data to be processed reach 24 times comparing with the FHD 8bit pixel video.

In order to process the large amount of data, 8K 60

frames per second in real time, the huge computation and memory bandwidth are needed. The proposed sub-system can give the solution for them.

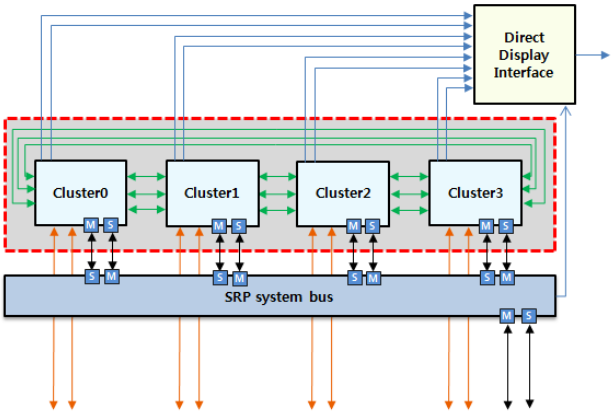


Fig. 1. Video post processing platform architecture

B. Proposed Platform Architecture

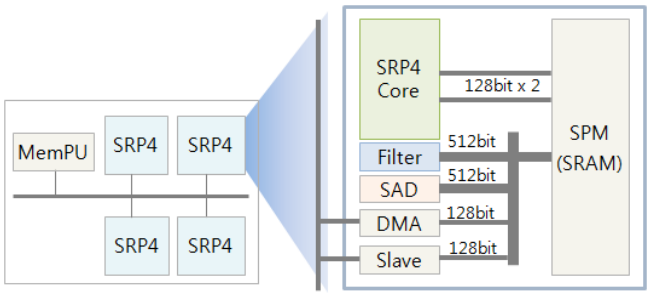
We propose a cluster-type post processing platform. The sub-system is composed of 4 clusters, one DDI (Direct Display Interface) block and bus, which is shown in Fig. 1.

Multi-clusters can support the data partitioning for parallel process and the data pipelining is possible between the clusters. Each cluster can post-process 1/4 of 8K video data in parallel. The eight bus signals are connected to external system bus directly to transfer DDR-SDRAM data fast. In order to proceed in real time on-the-fly processing of resolution up to 8K video, the size of the sub-system is increasing up to 57M G/C in 28nm process.

DDI block is responsible for display data transfer from the clusters to the external system. On-the-fly data transfer can be done by DDI without using DDR-SDRAM. Using DDI, it is possible to reduce the DDR-SDRAM bandwidth that huge data of 8K UHD video transfer to DDR-SDRAM- 60 frames of DDR-SDRAM writing and 60 frames of DDR-SDRAM reading per second.

As shown in Fig. 2 (a), one cluster consists of 4 SRPs, one MemPU and bus. MemPU supports the efficient data transfer between SRP and DDR-SDRAM. It has also function blocks to reduce the SRP calculation like clipping, bitwidth-change and sum of data.

Fig. 2 (b) shows the SRP4 (SRP version4) architecture. The SRP block gets the hybrid architecture – SRP core with H/W accelerators – in order to maximize the SRP operation because the amount of 8K data to be processed is huge compared to FHD (1920x1080l) data. While SRP is performing the operation set by the program, flexible H/W accelerators, Filter and SAD, can minimize the post processing time by executing in parallel the operation by the command of SRP.



(a) Cluster architecture (b) SRP4 architecture

Fig. 2. Cluster architecture & SRP4 architecture

3. PERFORMANCE

For real-time processing of image quality resolutions up to 8K, each cluster should post-process 60 frames per second or more of 4K video. MemPU can access eight DDR-SDRAMs at the same time and has a DRAM bandwidth of up to 224 frame/s (8K, YUV422 12bit pixel).

TABLE I
VIDEO ENGINE PERFORMANCE (YUV 422 12BIT PIXEL)

Resolution	DRAM bandwidth	Display bandwidth	Calculation
7680x4320	224 frm/s	165 frm/s	4.3 TOPS*

*TOPS : Tera Operations per second

The performance of the video engine will be explained fully in the full paper.

4. PLATFORM APPLICATIONS

Fig. 3 shows the block diagram of post processing after video decoding in current DTV system. When applying the platform that has been proposed, all the post processing blocks except for FRC (Frame Rate Conversion) and Scaler Noise reduction, Detail Enhancement, Contrast Enhancement, Color Enhancement (CE), and Black Management can be programmable by S/W.

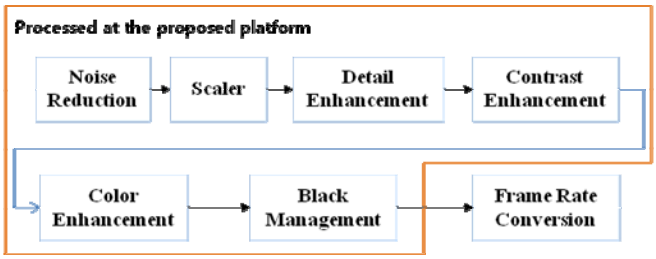


Fig.3. DTV Video Post Processing Block Diagram

For the video post processing, unlike such as standardized video decoder, the video quality enhancement algorithms are consistently improved.

(a) Original input image

(b) Output of post processing algorithm

Fig.4. Result of post-processing based on SRP platform

When applying the proposed platform, it is possible to respond to changes in the video post processing algorithm only by updating S/W. Further, when developing a new DTV, by simply changing the S/W without new SoC design, it can reduce the cost and development time.

The video sequence after post processing is shown in Fig. 4. By applying updated algorithms, the platform makes the improved image quality.

5. CONCLUSION

This paper proposes a world's first 8K video post processing platform based on SRP. The programmable video processing pipeline can process 4K/8K UHD images with real time and allows you to upgrade video quality without having to buy a new TV set.

The proposed sub-system has been embedded into Soc and new 8K UHD TV set using the programmable SoC is expected at CES2015 for the first time in the world.

References

[1] Ultra High Definition Television: Threshold of a new age". ITU. May 24, 2012. Retrieved July 31, 2012.

[2] "NHK and Mitsubishi Electric Corporation Successfully Develop World's First HEVC Encoder for 8K "Super Hi-Vision"". Finance (Yahoo). May 9, 2013. Retrieved May 9, 2013.