SRAM의 읽기 및 쓰기 동작을 위한 Assist Block

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Assist Block for Read and Write Operations of SRAM

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Abstract

Static Random Access Memory (SRAM) using CMOS technology has many advantages. It does not need to refresh every certain time, as a result, the speed of SRAM is faster than *Dynamic Random Access Memory (DRAM)*. This is the reason why SRAM is widely used in almost processors and system on chips (SoC) which require high processing speed. Two basic operations of SRAM are read and write. We consider two basic factors, including the accuracy of read and write operations and the speed of these operations. In our paper, we propose the read and write assist circuits for SRAM. By adding a power control circuit in SRAM, the write operation performed successfully with low error ratio. Moreover, the value in memory cells can be read correctly using the proposed pre-charge method.

1. Introduction

SRAM is a type of semiconductor memory that uses bi-stable latching circuits to store each bit. A typical SRAM cell is made up of six *metal–oxide–semiconductor field-effect transistors (MOSFETs) [1], [2]* (see Figure 1). Each bit in a SRAM is stored on four transistors (M_1, M_2, M_3, M_4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote “0” and “1”. Two additional access transistors M_5 and M_6 used to control the access to a storage cell during read and write operations. Besides six-transistor (6T) SRAM, other kinds of SRAM chips use 4T, 8T, 10T, or more transistors per bit.

An SRAM cell has two mainly states. It can be in read or write state. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The two different states work as follows:

Read operation - Assume that the content of the memory is “1”, stored at the transistor Q. The read cycle is started by pre-charging both the bit lines (BL and BLX) to a logical “1**”**. After that, the word line (WL) is changed to logical “1” and both access transistors M_5 and $M_6$are enabled. The second step occurs when the values stored in memory cells are transferred to the bit lines by leaving BL at its pre-charged value and discharging BLX through M_1 and M_5 to a logical “0**”**. On the BL side, the transistors M_4 and M_6 pull the bit line toward V_{DD}. If the content of the memory was “0**”**, the opposite would happen and BLX would be pulled toward “1**”** and BL toward “0”. Then these BL and BLX will have a small difference between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was “1**”** or “0**”**stored. The higher sensitivity of the sense amplifier, the faster the speed of read operation is.

Write operation - A write cycle is started by applying the value to be written to the bit lines. This is similar to applying a reset pulse to a latch, which causes the flip flop to change state. A “1**”** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in.

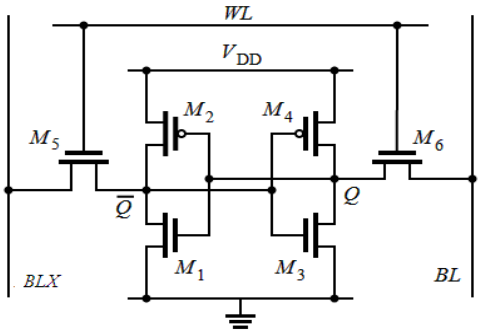


Figure 1. 6T bit-cell

The successful rate in read and write operations is an important parameter. Besides, we must consider how long it takes to finish one read and write cycles. Our proposed design improves the successful rate in read and write operation as well as decrease the read and write cycles by using the new pre-charge technology in read operation and adding the power control circuit in write operation.

2. Related work

A semiconductor memory device comprises a plurality of memory cells, including a holding circuit for holding memory data and a read-only output circuit for outputting a signal corresponding to the data held by the holding circuit. *Renesas Corp* [3] changes the length of the read-driven and read-access transistor. This length is longer than the gate length of transistors in the holding circuit.

Younghwi Yang [4] proposes a read-preferred SRAM cell with a write-assist circuit using the back-gate *extremely thin silicon-on-insulator (ETSOI)*. The proposed write-assist circuit minimizes the dynamic power overhead and satisfies a sufficient sigma cell in all cells during the read and write operations.

ETSOI is one of the attractive candidates for 22-nm and beyond technology nodes to resolve the problems of planar bulk MOSFETs. Figure2shows a schematic cross-sectional view of the ETSOI structure with back gate

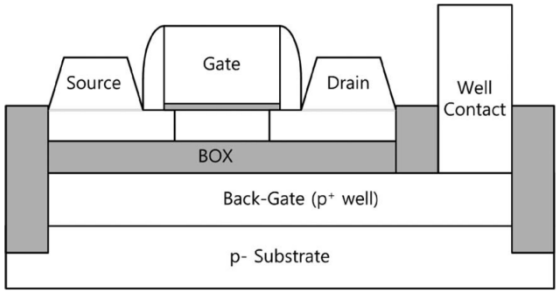


Figure 2. Schematic cross-sectional view of ETSOI structure with the back gate

3. Proposed architecture

In our design, we divide memory into four blocks (see Figure 3). These blocks with a dedicated role are easy for us to design, simulate and debug. The first block is ***control block*– CTL.** This block generates control signals to control all other blocks. The pulse from CTL block used to synchronize the read and write operations. The second one is ***address decoder block – XDEC*** *which* decodes address signal to determine the location of memory cells. ***Memory block – CORE*** is the main block of the memory. It includes a large number of memory cells (depend on the capacity of the memory).Finally, the fourth block is ***input-output block – IO*** consisting of important circuits such as buffers, amplifiers, latches, etc. which relate to read and write operations.

CTRL Block	**CORE Block**
XDEC Block	**IO Block**

Figure 3. General architecture of SRAM

Two important operations of the memory are read and write. In read operation, the signal from CTRL block creates the internal pulse to control the read operation. The address signal is entered address port A[10:1] to choose a memory cell. The write-allowed signal WEN_B is set at logic level “1”. The value in the memory cell pulls BL (if read “0” from memory cell), or BLX (if read “1” from memory cell) to logic level “0”.When the offset between BL and BLX reaches a certain value, the amplifiers is activated (the SAEN signal is pulled up to level “1”). The data from memory cell is driven to output port DO[63:0]
In write operation, the chip-select signal CEN_B, the write signal WEN_B, address signal A[10:0] and data signal are latched before the increase edge of CLK signal. These signals are constant in a certain time. BL/BLX is pulled down so that the value of memory cell is changed. The amplifier block does not work in write operation.

We set BL/BLX to level “1” and SL/SLX to level “0” (see Figure 4) instead of using the traditional pre-charge technology which sets BL/BLX to a reference level (V_{ref}) in read operation. Furthermore, a circuit which can choose the power supply is added into IO block to improve successful rate in write operation.

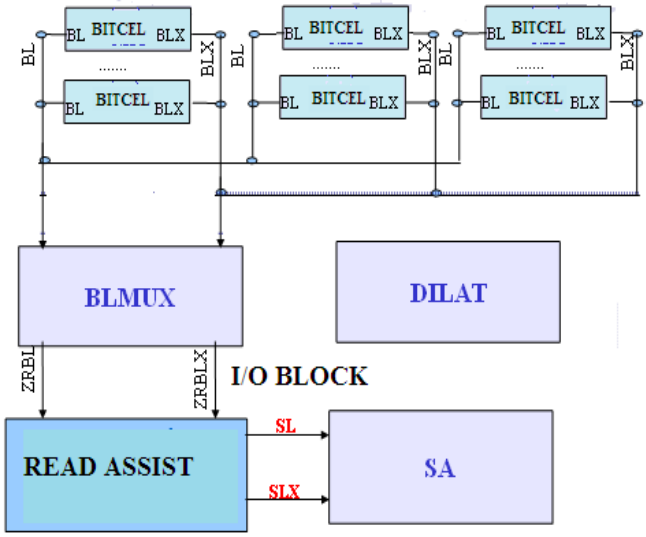


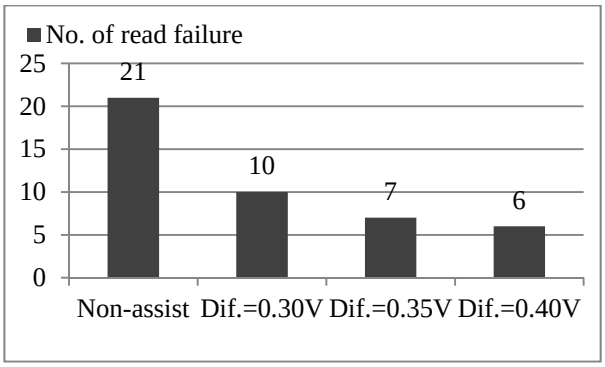
Figure 4. Position of read assist in I/O block

4. Performance Evaluation

We use Cadence software to design the memory circuits [5]. In addition, HSPICE software supports simulation in various states and frequency domain [6]. Therefore, we use these software and Monte Carlo simulation to estimate our design.

Monte Carlo method [7] is a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results.

In our simulation, we repeat 1000 times randomly.



Dif. = VDD – VBL. Non-assist is used in [3] and [4]

Figure 5. Number of read failure (per 1000)

The simulation result shows that when using the assist block, the number of failure in write operation decreases dramatically by 58% compared to non-assist block (see Figure 5). Moreover, the number of failure in read operation declines by 52% (VDD – VBL = 0.1V) and 71% (VDD-VBL = 0.3V) (see Figure 6).

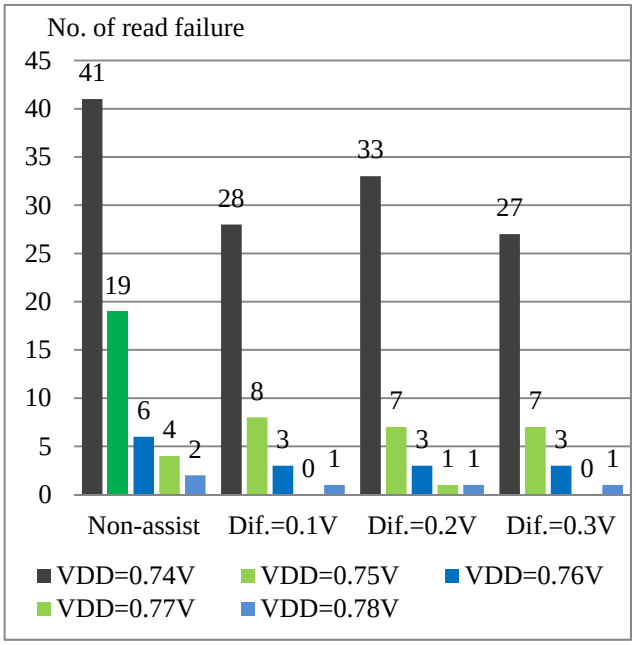


Figure 6. Number of write failure (per 1000)

5. Conclusion

In this paper, we introduce a new technology to support read and write operations of SRAM. The accuracy in these operations is improved significantly. We also decrease the time in read and write operations. Thus, the memory performance is improved.

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