Improvement of carrier transport in silicon MOSFETs by using h-BN decorated dielectric

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Abstract

We present a comprehensive study on the integration of h-BN with silicon MOSFET . Temperature dependent mobility modeling is used to discern the effects of top-gate dielectric on carrier transport and identify limiting factors of the system. The result indicates that coulomb scattering and surface roughness scattering are the dominant scattering mechanisms for silicon MOSFETs at relatively low temperature. Interposing a layer of h-BN between SiO_2 and Si effectively weakens coulomb scattering by separating carriers in the silicon inversion layer from the charged centers as 2-dimensional h-BN is relatively inert and is expected to be free of dangling bonds or surface charge traps owing to the strong, in-plane, ionic bonding of the planar hexagonal lattice structure, thus leading to a significant improvement in mobility relative to undecorated system. Furthermore, the atomically planar surface of h-BN also suppresses surface roughness scattering in this Si MOSFET system, resulting in a monotonously increasing mobility curve along with gate voltage, which is different from the traditional one with a extremum in a certain voltage. Alternatively, high-k dielectrics can lead to enhanced transport properties through dielectric screening. Modeling indicates that we can achieve even higher mobility by using h-BN decorated HfO_2 as gate dielectric in silicon MOSFETs instead of h-BN decorated SiO_2.