Multilevel Modular Converter의 개선된 시뮬레이션 방법

원진, 파자르, 이혜연, 조진상, 장수형
LS산전

A kind of Improvement Simulation Method for Multilevel Module Converter

Zhen Yuan, Fajar Sastrowijoyo, Hyeyeon Lee, Jinsang Jo, Suhyeong Jang
LSIS

ABSTRACT

Multilevel Voltage Source Converter HVDC presents a new method for the energy transmission, The multilevel requires the converter bridge includes more than 100 converter modules, for the EMT simulation file, the simulation time increases to several hours; it can depress the research process[1]. In the paper, author describes a method to simulate the multilevel arm based on time varying equivalent. The result shows the extremely calculation time reduced with almost the same accuracy.

1. Introduction

Now in the world, the topology of the VSC HVDC includes three types: Two level converter, Three level converter and modular multi level converter. MMC (modular multi level converter) proposed offers the following advantages: Low generation of harmonics, low HF noise; No capacitor at DC terminals, allowing for excellent dynamic behavior.

However, since the level of MMC topology is more than 200 in the practical utilization, the large number of switching elements in the MMC introduces a challenge for modeling the converter. Using the PSCAD built in switching elements, the admittance matrix which has a size equal to the total number of nodes can make the simulation time to several hours. It is necessary to introduce a new approach to modeling the MMC, using the method of Dommel's algorithm[2]. It partitions the solution into two parts, with the external network solution being implemented in the main ENT solver, each phase of the MMC is interfaced as a specially designed Thevenin equivalent, thereby greatly reducing the number of nodes. Mathematically, the method is exactly equivalent to conducting an EMT simulation in the traditional manner, but can be implemented with much reduced computational effort while retaining the accuracy.

2. A Kind of Improvement Simulation Method for Multilevel Module Converter

2.1 MMC Topology Description and Analysis

The typical structure of a MMC is shown in Fig. 1, and the configuration of a Sub Module (SM) is given in Fig. 2.Each SM is a simple chopper cell composed of two IGBT switches, two anti parallel diodes and a capacitor C. Each phase leg of the converter has two arms, each one constituted by a number N of SMs.

The switching sequence is controlled so that at each instant only N SMs (i.e. half of the 2N SMs of a phase leg) are in the on state. As an example, if at a given instant in the upper arm SMs from 2 to N are in the on state, in the lower arm only one SM will be in on state. Equal voltage sharing among the capacitor of each arm can be achieved by a selection algorithm of inserted or bypassed SMs during each sampling period of the control system.

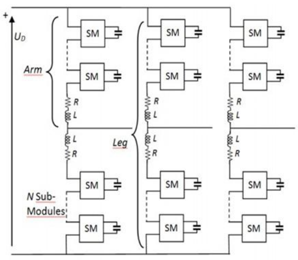

Fig. 1 Three-phase MMC converter topology

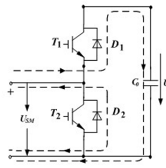

Fig. 2 Sub-Module scheme

2.2 Equivalent Module Modeling

The converter consists of three phase units, each with upper and lower arm. Each arm has a modular structure with a number of series connected power sub modules. Here the IGBT switches can be treated as two state resistive devices. When the IGBT is turn on status, the resistor is chosen to be 0.01Ω, When the IGBT is turn off status, resistor is chosen to be 1MΩ. Since the parallel connection of an IGBT and a diode acts as a bidirectional switch and only one device is conducting at a given instance, the pair is still considered as a single two state resistance. Using the trapezoidal integration method, the capacitor can be represented as an equivalent voltage source and a resistor, see Fig 3.

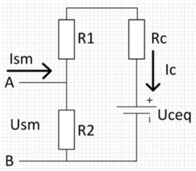

Fig. 3 Equivalent circuit of sub-module

Using the trapezoidal integration method, the arm output voltage can as below:

$$u_{br}(t)=\sum_{i=1}^{n}u_{sm}^{i}(t)=(\sum_{i=1}^{n}R_{smeq}^{i})i_{br(t)}+\sum_{i=1}^{n}u_{smeq}^{i}(t-\triangle t) \quad (1)$$

$$=R_{br}i_{br}(t)+u_{br}(t-\triangle t)$$

2.3 Simulation

In the simulation, an improvement of the Dommel's algorithm is multistep hierarchical approach partitions the network into smaller sub networks and solves the admittance problem for each separately. The size of each of the admittance matrices is much smaller than that of the admittance matrix of the full network, which can lead to a reduction in simulation time.

To verify the effectiveness of the topology mechanism and MMC modeling, a 31 level two terminal MMC HVDC system was modeled in PSCAD/EMTDC, whose structure is shown in Fig. 4.

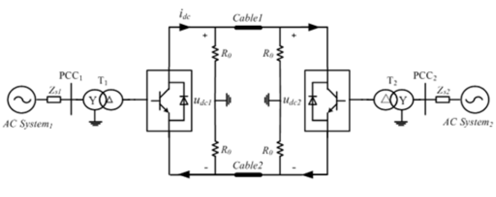

Fig. 4 MMC Simulation Structure

In this simulation, the simulation progress is separated into two part, start up part and operation part.

From the initial state to 4.0s, all the 4 controlled variables of MMC (both rectifier and inverter sides) are fixed to their rated values, and at 4.0s, the active power order in inverter side changes from 1p.u. to 0.9 p.u., the control effects of the designed controllers can be seen from Fig. 5 to Fig. 6.

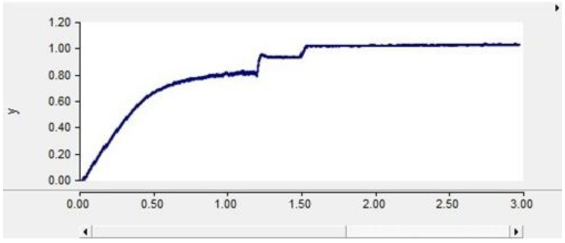

Fig. 5 DC start-up voltage [pu]

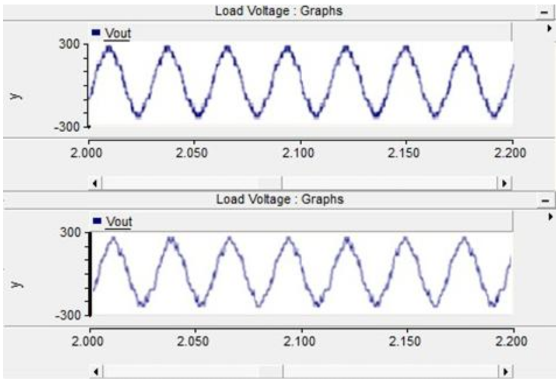

Fig. 6 Compared outout voltage [kV]

3. Conclusion

The simulation results above indicated that the proposed modeling method can be simulated in a satisfied time. In Fig 6, is the two simulation method result compared. The above one is the improvement model invert side AC voltage, and the below one is the PSCAD library built up model invert side AC voltage. The waveforms almost are similar.

Using this equivalent circuit model, the running time is almost 15s. If using the PSCAD library model, the running time can be more than 120 seconds. And more, we do more interesting test in lab, we construct the 151 level using the PSCAD library model, the finish time is the next day. Also using our improvement simulation method, the running time can be unimaginably to 250 seconds.

We can conclude, the improvement simulation method result is not worse than the PSCAD library built up model, but the running time is totally different. The method can drastically improve our research progress.

참 고 문 헌

[1] Udana N. G, Aniruddha M. G, Rohitha P. J Modeling of Modular Multilevel HVDCConverters (MMC) on Electromagnetic Transient Simulation Programs[J]. IEEE Transactions on power delivery, VOL. 26, NO. 1, January 2011

[2] Dommel H W. Digital computation of electromagnetic transients in single and multi phase networks [J]. IEEE Transaction on Power App. 1969, 88 (04): 388 399