RCD Snubber Design and Analysis using Resonance Coordinate

Shan-Mei Li and Gwan-Bon Koo

Fairchild Korea Semiconductor, 82-3, Dodang-dong, Wonmi-gu, Bucheon-si, Gyeonggi-do, 420-711, KOREA

Abstract

An approach to design and analyze an RCD snubber for flyback converters will be introduced. The resonance coordinate provides an easy way to understand the transient period of the switch turn-off and helps to design and analyze the RCD snubber easily. An example of analyzing RCD snubber losses for 40W prototype will be given and experimented to show the effectiveness of the suggested method.

1. Introduction

Commercially, the flyback converter is widely used due to its light weight and low cost. However it has a serious problem: hard switching operation of the main switch, which results in a high voltage surge and oscillation across the switch. The voltage stress of the main switch is the sum of input voltage V_{in}, reflected output voltage nV_{out} and voltage spike caused by the leakage inductance. The most widely used method for reducing voltage spike is using an RCD snubber network. If the snubber resistance R_{sn} is decreased, the snubber capacitor voltage V_{sn} is also decreased; however, the power loss caused by R_{sn} is increased. So using the RCD snubber, a trade-off is needed between voltage stress (the sum of V_{in} and V_{sn}) and efficiency. So an optimal RCD snubber design is necessary.

This paper deals with the conventional analysis of the voltage spike caused by the leakage inductance. Then an easy analyzing method in resonance coordinate will be introduced for further analysis. For optimal design, snubber current will be analyzed in resonance coordinate. The validity of the introduced analysis method using resonance coordinate will be evaluated with an example of analyzing RCD snubber losses for 40 W prototypes.

2. RCD snubber design and analysis

2.1 General method of RCD snubber design

The RCD snubber circuit is used to clamp the voltage spike caused by the resonance between leakage inductance and output capacitance of the switch MOSFET to protect MOSFET with a limited breakdown voltage rating. To describe the operational principles to design the RCD snubber, there are a couple of assumptions;

(1) $V_{sn} > nV_{out}$, and V_{sn} is almost constant due to the large C_{sn};

(2) $C_{DS} = C_{OSS} + C_{TRANS}$, and is constant regardless of $v_{DS}(t)$;

(3) No secondary side leakage inductance, thus $i_{DS}(t)$ can be changed into the secondary side diode current instantaneously when primary switch Q1 turns off, where C_{sn} is the snubber capacitance, C_{DS} is the effective capacitance between drain and source of the main switch, C_{OSS} is the output capacitance of the switch MOSFET, C_{TRANS} is the effective capacitance between the primary terminals of the transformer, $v_{DS}(t)$ is the voltage across the main switch, $i_{DS}(t)$ is the current flowing through the main switch, and Q1 is the main switch.

When switch Q1 turns off, the primary current charges C_{OSS} of Q1(discharges C_{TRANS} of the transformer at the same time). When C_{OSS} is charged up to V_{in}+nV_{out}, the secondary side diode turns on and the energy is transferred to the secondary side, and C_{OSS} is charged continuously, because the leakage inductance L_{lk} still has some remnant energy. When $v_{DS}(t)$ of Q1 increases to V_{in}+V_{sn}, the snubber diode D_{sn} turns on and $v_{DS}(t)$ is clamped to V_{in}+V_{sn}. When D_{sn} conducts, the voltage across L_{lk} is V_{sn}-nV_{out}, and the turn-on time of $D_{sn}(t_s)$ can be obtained as follows:

$$t_s = \frac{L_{lk} \times I_{peak}}{V_{sn} - nV_{out}}. \tag{1}$$

where I_{peak} is the peak drain current just before the switch Q1 turns off. The power dissipation in the snubber network (P_{sn}) is

$$P_{sn} = \frac{1}{2} \times L_{lk} \times I_{peak}{}^2 \times f_{sw} \times \frac{V_{sn}}{V_{sn} - nV_{out}} = \frac{V_{sn}{}^2}{R_{sn}}. \tag{2}$$

Therefore, the snubber resistor R_{sn} can be obtained as:

$$R_{sn} = \frac{V_{sn}{}^2}{\frac{1}{2} \times L_{lk} \times I_{peak}{}^2 \times f_{sw} \times \frac{V_{sn}}{V_{sn} - nV_{out}}}. \tag{3}$$

However, the peak drain current is reduced somewhat after stepping a couple of stages of L-C resonance. Therefore, the above equation might mislead an over-designed system. So I_{peak} of Eq. (1) should be changed with the peak current of snubber ($I_{pk,sn}$).

Let's find out $I_{pk,sn}$ using resonance coordinate to avoid an over design of the RCD snubber in the following section.

2.2 RCD snubber design and analysis in resonance coordinate

An RCD snubber design will be done in resonance coordinate in this chapter. To design the snubber only, there is no need to analyze the whole flyback operational modes. Figure 1 shows the typical $v_{DS}(t)$ of the switching MOSFET in flyback converters.

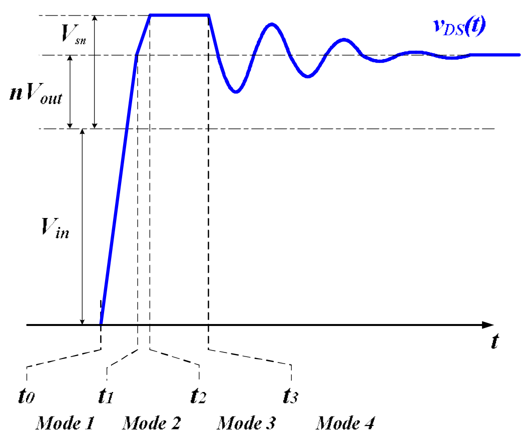

Figure 1. $v_{DS}(t)$ after switch turns off

In Mode 1, the current in the inductors (L_{lk} and L_m) charges C_{DS} until its voltage reaches V_{in}+nV_{out}, where L_m is the magnetizing inductance of the transformer. In Mode 2, by the resonance between C_{DS} and L_{lk}, the voltage on C_{DS} increases up to V_{in}+V_{sn} at the end of this mode.

2.2.1 Equations for the Peak Drain Current

i_{DS}(t) and v_{DS}(t) can be plotted in the resonance coordinate as shown in Figure 2 during Modes 1~4.

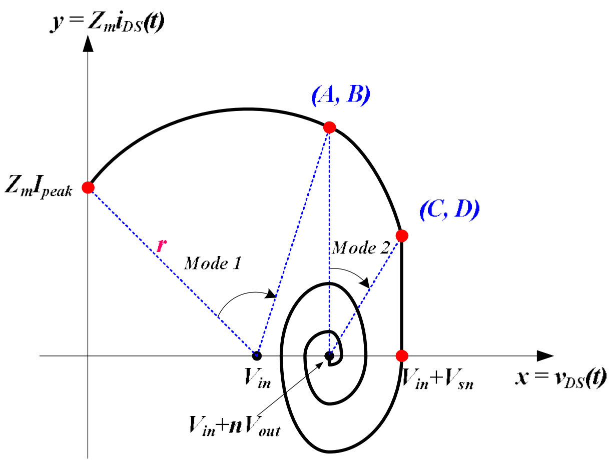

Figure 2. Mode analysis in resonance coordinates

Mode 1. It is a circle with the origin at (V_{in}, 0) and the kick-off point at (0, Z_mI_{peak}). From Mode 1 of Figure 2,

$$(x - V_{in})^2 + y^2 = V_{in}^{\ 2} + (Z_m I_{peak})^2 \tag{4}$$

where Z_m is the characteristic impedance of L_m and C_{DS}, √(L_m/C_{DS}).

Mode 2. It is an ellipse with the origin at (V_{in}+nV_{out}, 0) and the kick-off point at (A, B). And the circle is changed into an ellipse by coordinate mapping. From Mode 2 of Figure 2,

$$\left(x - (V_{in} + nV_{out})\right)^2 + \left(\sqrt{\frac{L_{lk}}{L_{lk} + L_m}} \times y\right)^2 = \left(\sqrt{\frac{L_{lk}}{L_{lk} + L_m}} \times B\right)^2 . \tag{5}$$

From Eqs. (4) and (5), $I_{pk,sn}$ (point D) is obtained as

$$I_{pk,sn} = \sqrt{\frac{C_{DS}}{L_{lk} + L_m}\left\{V_{in}^{\ 2} + \left(Z_m I_{peak}\right)^2 - \left(nV_{out}\right)^2 - \frac{L_{lk} + L_m}{L_{lk}}\left(V_{sn} - nV_{out}\right)^2\right\}} . \tag{6}$$

The Eq. (6) is calculated with an assumption that there is no leakage inductance in snubber network that i_{DS}(t) is right the same as the $I_{pk,sn}$ when snubber conducts. i_{sn}(t) increases with a slope determined by parasitic inductance($L_{lk,sn}$) which exists in the snubber network for a really short time when v_{DS}(t) reaches V_{in}+V_{sn}. So real snubber peak current I_{pk,sn_r} is smaller than $I_{pk,sn}$ of Eq. (6). Considering $L_{lk,sn}$, I_{pk,sn_r} is calculated as

$$I_{pk,sn\_r} = \frac{I_{pk,sn}}{1 + \frac{L_{lk,sn}}{L_{lk}}} . \tag{7}$$

To obtain the correct equations for the power loss and R_{sn} in the snubber network, I_{peak} of Eqs. (2) and (3) should be replaced by I_{pk,sn_r} of Eq. (7).

According to Eqs. (2), (6), and (7), for reducing snubber loss, L_{lk}, I_{peak}, and f_{sw} should be reduced, and C_{DS} should be increased.

2.2.2 Evaluation of the optimized snubber by experimental results

When a system operates with the calculated R_{sn} (23.5 kΩ) using the conventional method, key waveforms of i_{DS}(t) and i_{sn}(t) and v_{DS}(t) are obtained as Figure 3.

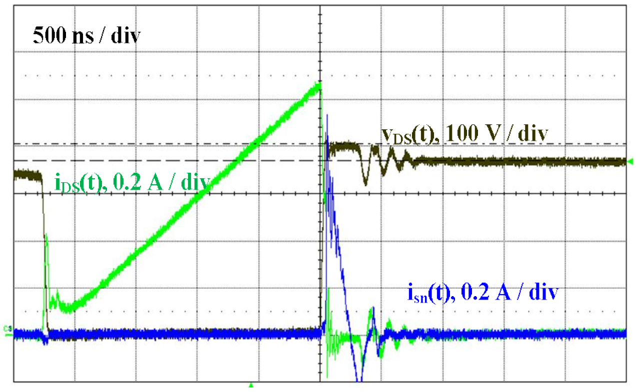

Figure 3. Key waveforms (Test conditions: V_{in}=300 Vdc, P_{out}=40 W, V_{out1}=15 V, I_{out1}=2 A, V_{out2}=5 V, I_{out2}=2 A, L_{lk}=5 uH, L_m=600 uH, C_{DS}=170 pF, $L_{lk,sn}$=0.6 uH)

The measured values for the current, voltage, and switching frequency are as follows: I_{peak}=1.058 A, I_{pk,sn_r}=0.916 A, f_{sw}=64 kHz, V_{sn}=101 V, nV_{out}=70 V. The calculated I_{pk,sn_r} is 0.941 A using Eqs. (6) and (7), which is a little bit higher than the measured I_{pk,sn_r}. But the calculated I_{pk,sn_r} is close to the measured I_{pk,sn_r}, compared to I_{peak}. Accordingly, the power losses P_{sn} calculated based on R_{sn} and I_{pk,sn_r} are closer than the case of I_{peak}. They are P_{sn_Rsn}=0.434 W and P_{sn_Ipk,sn_r}=0.462 W respectively, while P_{sn_Ipeak}=0.584 W, which is much larger than real P_{sn}. The difference of P_{sn} calculated based on I_{peak} and I_{pk,sn_r} is determined as Eq. (8).

$$\Delta P_{sn} = \frac{1}{2} \times L_{lk} \times f_{sw} \times \frac{V_{sn}}{V_{sn} - nV_{out}} \times (I_{peak}^{\ 2} - I_{pk,sn\_r}^{\ 2}) . \tag{8}$$

If P_{sn} is over estimated using I_{peak}, R_{sn} will be over designed. For more optimal design, R_{sn} should be chosen based on I_{pk,sn_r} instead of I_{peak}, and P_{sn} will decrease and R_{sn} will increase .

3. Conclusion

We can find out the exact snubber peak current using the resonance coordinate. Normally, R_{sn} is chosen based on I_{peak} for approximation and accordingly the R_{sn} is an over-designed value, because P_{sn} is over estimated. Using I_{pk,sn_r} we can get a more exact and smaller estimated P_{sn} and larger R_{sn} consequently.

However, the modified I_{pk,sn_r} is almost same as the original I_{peak}, if the characteristic impedance of Z_m is very large. The smaller the original I_{peak}, the more gap between I_{peak} and I_{pk,sn_r}. As a result, the modified method is useful in low power level power supply unit.

Reference

[1] Fairchild Semiconductor Application Note "AN-4137, Design Guidelines for Off-line Flyback Converters Using FPS".