The Development of High Power 3 Level Inverter based on FPGA

Xiao-Lin Peng, Bayasgalan.D, Ji-Su Ryu, Sang-Ho Lee
Seoho Electric Co. Ltd
900-3, Hogye 2-dong, Dongan-gu Anyang-city, Kyunggi-do, 431-836, KOREA

Abstract: Three-level neutral point clamping (NPC) converter has been widely applied in high power drive system. And in this paper, a novel method is proposed to realize this algorithm based on FPGA, And the system is consist of two parts, the DSP part and FPGA part, the DSP part includes the control algorithms and the FPGA part works to generate and putout 12 PWM pulses. And the system is tested and verified using both simulation and experimentation.

Keywords: induction motor, 3-level inverter, high power, FPGA, Neutral point clamped, voltage balance.

I. INTRODUCTION

The IGBTs bridge of the 3-level neutral point clamping (NPC) converter was provided in some textbooks, and it is follow as Figure 1 which helps to understand the structure and algorithm.

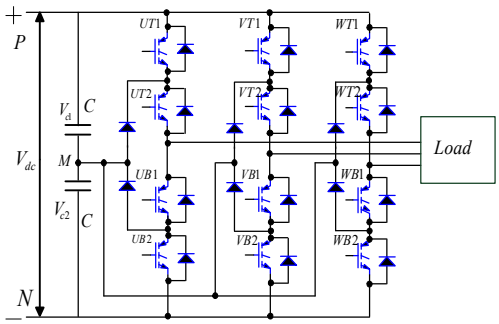


Figure 1: IGBTs Bridge

Where:

P: Positive of the DC link;
N: Negative of the DC link;
M: Natural point;

In the system, the DC-link voltage Udc = 1820V. And the 12 IGBTs are driven by 12 PWM pulses, and there are 4 PWM pulses in the same lag-bridge are generated by the same phase modulation wave. In other words, the IGBTs UT1, UT2, UT3, UT4 : VT1,VT2,VT3,VT4 and WT1, WT2, WT3, WT4 are matched to A , B and C phase voltage.

And the control system is consist of two part: the DSP part and FPGA part, the DSP part includes the control algorithms, such as V/f, vector control, and sensor less control, and output the modulation signal; and the FPGA part includes the neutral point potential balancing (NPPB) algorithm and PWM pulse generator, also this part receives the modulation signal by bidirectional data bus, then generate and putout 12 PWM pulses. And this paper focus on the algorithm and the realize method in the FPGA part, and then obtained experimental results.

II. MODULATION STRATEGY

2.1 The modulation algorithm

There are 4 algorithms in the FPGA, 3phase to 2 phase conversion, the space-vector modulation (SVP), the neutral point potential balancing algorithm (NPPB), dead time compensation algorithm. And the first algorithm was provided in some textbook, and we focus on other algorithms.

The strategy [2] was applied in the SVP algorithm, and the 3 phase modulation wave can be described as:

$$v_{ip} = \frac{v_i - mix(v_a, v_b, v_c)}{2}, v_{in} = \frac{v_i - \max(v_a, v_b, v_c)}{2}; i = \{a, b, c\} \quad (1)$$

where: v_{ip} and v_{in} are positive and negative part of the 3 phase modulation wave, and the positive modulation wave compare with the positive carrier wave and putout the PWM pulse to drive the IGBTs UT1,UB1;VT1,VB1;WT1,WB1 . And also the negative modulation wave compare with the negative carrier wave, then the output PWM pulse to drive the other 6 IGBTs . And an offset value:

$$\Delta U_{NPPB} = k_p |\Delta U_{dc}| * sign(\Delta U_{dc}) * sign(v_{ip} + v_{in} - 1). \quad (2)$$

was added to the modulation wave v_{ip} and v_{in} to resolve the neutral point potential balancing (NPPB) problem and the difference of the DC-link is less than 8V after applied this balance algorithm when driving motors (Udc = 1820V in the experiment) .

And in the dead time composition, another offset value ΔU_{DT} was also add to the modulation wave.

$$\Delta U_{DT} = (T_{DT} + T_{ON} + T_{OFF}) * U_{dc} * (1/T_{SS}) \quad (3)$$

Where: T_{DT} is the dead time, T_{ON} and T_{OFF} is the IGBT turn-on and turn-off time. U_{dc} is the peak of the carrier wave. T_{SS} is the interrupt cycle.

2.2 PWM generation method

In this system, a TMS320F2407 works the task as send or receive and some control algorithm. And The2r/3r transform, oscillation suppression, Dead Time compensation, Zero

sequence injection, NPPB algorithms work in the interrupt BLOCK in FPGA, it looks like a real DSP. This software DSP's interrupt frequency is 2kHz，offered by a counter. And using VHDL language to realize algorithm in the interrupt BLOCK, the result is surely because these algorithm work in the same clock frequency. The bidirectional data bus includes 8 bit data bus and 13 bit address bus, to realize high speed communication between DSP and FPGA. And the synchronous signal that come from DSP works to clear the carrier counter and latch the result of the interrupt BLOCK in every DSP interrupt cycle. So the key part in this project is to build the interrupt BLOCK, and the time order of the data feedback.

III. Experimental Results

In this work, experiments were done using an 110kW motor. The IGBT power converter was droved by TI TMS320F2407 and ALTERA FPGA a 32 bit microprocessor. The PWM frequency in overall system was 1k Hz. However, this frequency can set from keypad. The voltage and current adopt hardware RC filters. And have an experiment in the V/F control, sensor less control and parameter identification.

In the experimental, the motor nameplate: Power output: 110.0kW; Line voltage: 1140V; pole: 4; Supply frequency: 50Hz; Rated speed: 1489rpm.

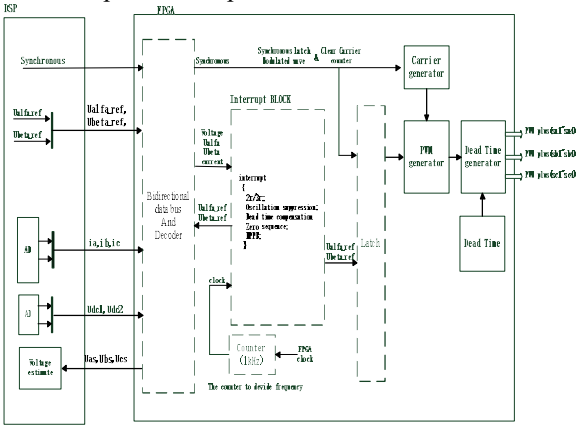


Figure 3: software structure in FPGA

3.1 V/f control. The voltage-frequency curve (test in the liner reference):

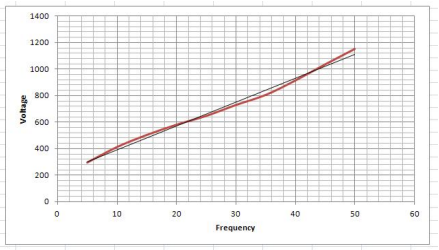
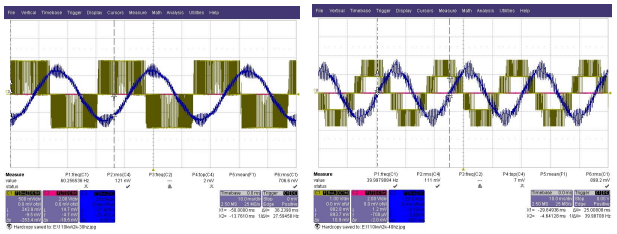


Figure 4: Voltage-Frequency curve

X-axis: output voltage; Y-axis: reference frequency; and the red one: real voltage-frequency curve, the back one: linear curve

3.2 Sensor less control. The current wave



(a) (b)

Figure 5: The current wave

The current wave (a) and (b) test in the 893rpm and 1192rpm, and blue one is a phase current wave, the yellow one is line voltage Uab.

3.3 Motor parameter identification.

In the development of parameter identification, the 2-level inverter's test result was considered as the standard value. And there are 3 times test and have an analysis in the stability by the average value and average variance value.

Table3: 3-level motor parameter identification

	1st	2nd	3td	AVG	STDEV
Rs0	58.806	70 906	58.806	62.84	6.985723
Rs1	84.840	96.629	84.840	88.77	6.806618
Rr	26.624	25.698	19.286	23.87	3.996503
Ls	132.95	140.43	129.93	134.4	5.403278
Lr	131.58	139.10	128.60	133.1	5.406152
Lsigma	5.4711	5.4627	5.4460	5.46	0.012739

IV. Conclusion

This paper presented a new method to realize the Three-level neutral point clamping (NPC) converter based on FPGA. And the software applied the mature techniques in the DSP part and reliable structure and algorithms in FPGA part. And the system, although the complexity of the algorithm is not negligible, works stably and have a good performance in motor parameter identification and sensor less control for large power motor.

And there is some improvements in the low frequency and parameter identification algorithm and the method also reveal some inspiration in the High Power 3 Level Inverter aspects.

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