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Graphene for MOS Devices

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Graphene has attracted much attention for future nanoelectronics due to its superior electrical properties. Owing to its extremely high carrier mobility and controllable carrier density, graphene is a promising material for practical applications, particularly as a channel layer of high-speed FET. Furthermore, the planar form of graphene is compatible with the conventional top-down CMOS fabrication processes and large-scale synthesis by chemical vapor deposition (CVD) process is also feasible. Despite these promising characteristics of graphene, much work must still be done in order to successfully develop graphene FET. One of the key issues is the process technique for gate dielectric formation because the channel mobility of graphene FET is drastically affected by the gate dielectric interface quality. Formation of high quality gate dielectric on graphene is still a challenging. Dirac voltage, the charge neutral point of the device, also strongly depends on gate dielectrics. Another performance killer in graphene FET is source/drain contact resistance, as the contact resistant between metal and graphene S/D is usually one order of magnitude higher than that between metal and silicon S/D. In this presentation, the key issues on graphene-based FET, including organic-inorganic hybrid gate dielectric formation, controlling of Dirac voltage, reduction of source/drain contact resistance, device structure optimization, graphene gate electrode for improvement of gate dielectric reliability, and CVD graphene transfer process issues are addressed.

Keywords: graphene FET

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Optoelectronic and electronic applications of graphene

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Graphene is expected to have a significant impact in various fields in the foreseeable future. For example, graphene is considered to be a promising candidate to replace indium tin oxide (ITO) as transparent conductive electrodes in optoelectronics applications. We report the tunability of the wavelength of localized surface plasmon resonance by varying the distance between graphene and Au nanoparticles [1]. It is estimated that every nanometer of change in the distance between graphene and the nanoparticles corresponds to a resonance wavelength shift of ~12 nm. The nanoparticle-graphene separation changes the coupling strength of the electromagnetic field of the excited plasmons in the nanoparticles and the antiparallel image dipoles in graphene. We also show a hysteresis in the conductance and capacitance can serve as a platform for graphene memory devices. We report the hysteresis in capacitance-voltage measurements on top gated bilayer graphene which provide a direct experimental evidence of the existence of charge traps as the cause for the hysteresis [2]. By applying a back gate bias to tune the Fermi level, an opposite sequence of switching with the different charge carriers, holes and electrons, is found [3]. The charging and discharging effect is proposed to explain this ambipolar bistable hysteretic switching.

References

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Keywords: graphene