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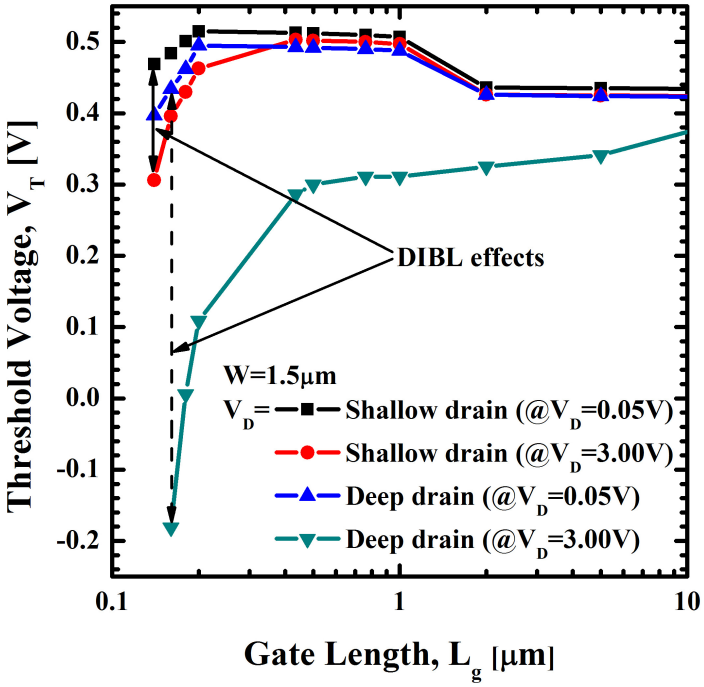
Comparison of Drain-Induced-Barrier-Lowering (DIBL) Effect by Different Drain Engineering

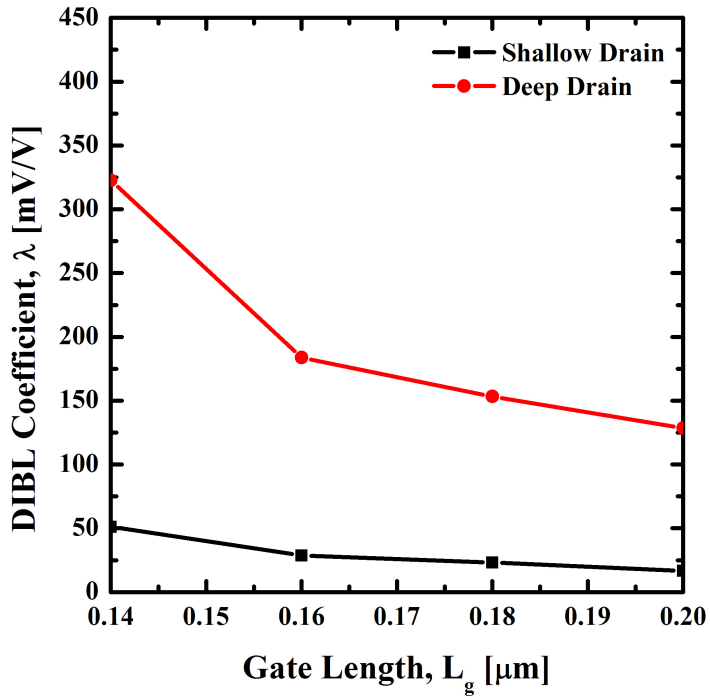
Byoungseon Choi, Pyungho Choi, Byoungdeog Choi

School of Information and Communication Engineering, Sungkyunkwan University

We studied the Drain-Induced-Barrier-Lowering (DIBL) effect by different drain engineering. One other drain engineering is symmetric source-drain n-channel MOSFETs (SSD NMOSs), the other drain engineering is asymmetric source-drain n-channel MOSFETs (ASD NMOSs). Devices were fabricated using state of art 40 nm dynamic-random-access-memory (DRAM) technology. These devices have different modes which are deep drain junction mode in SSD NMOSs and shallow drain junction mode in ASD NMOSs. The shallow drain junction mode means that drain is only Lightly-Doped-Drain (LDD). The deep drain junction mode means that drain have same process with source. The threshold voltage gap between low drain voltage (V_D=0.05V) and high drain voltage (V_D=3V) is 0.088V in shallow drain junction mode and 0.615V in deep drain junction mode at 0.16 μ m of gate length. The DIBL coefficients are 26.5 mV/V in shallow drain junction mode and 205.7 mV/V in deep drain junction mode. These experimental results present that DIBL effect is higher in deep drain junction mode than shallow drain junction mode. These results are caused that ASD NMOSs have low drain doping level and low lateral electric field.

Keywords: Asymmetric source-drain MOSFET, Drain-induce-barrier-lowering (DIBL), Drain engineering


Threshold Voltage, V_T [V]
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
0.1
1
10
Gate Length, L_g [μm]
DIBL effects
W=1.5μm
V_D=
Shallow drain (@V_D=0.05V)
Shallow drain (@V_D=3.00V)
Deep drain (@V_D=0.05V)
Deep drain (@V_D=3.00V)


DIBL Coefficient, λ [mV/V]
450
400
350
300
250
200
150
100
50
0
0.14
0.15
0.16
0.17
0.18
0.19
0.20
Gate Length, L_g [μm]
Shallow Drain
Deep Drain