TT-P041

Charge Pumping Measurements Optimized in Nonvolatile Polysilicon Thin-film Transistor Memory

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With the NAND Flash scaling down, it becomes more and more difficult to follow Moore's law to continue the scaling due to physical limitations. Recently, three-dimensional (3D) flash memories have introduced as an ideal solution for ultra-high-density data storage. In 3D flash memory, as the process reason, we need to use poly-Si TFTs instead of conventional transistors. So, after combining charge trap flash (CTF) structure and poly-Si TFTs, the emerging device SONOS-TFTs has also suffered from some reliability problem such as hot carrier degradation, charge-trapping-induced parasitic capacitance and resistance which both create interface traps. Charge pumping method is a useful tool to investigate the degradation phenomenon related to interface trap creation. However, the curves for charge pumping current in SONOS TFTs were far from ideal, which previously due to the fabrication process or some unknown traps. It needs an optimization and the important geometrical effect should be eliminated. In spite of its importance, it is still not deeply studied. In our work, base-level sweep model was applied in SONOS TFTs, and the nonideal charge pumping current was optimized by adjusting the gate pulse transition time. As a result, after the optimizing, an improved charge pumping current curve is obtained.

Keywords: Charge pumping, Poly-Si TFTs, SONOS