Floating Power Supply Based on Bootstrap Operation for Three-Level Neutral-Point-Clamped Voltage-Source Inverter

Nguyen Qui Tu Vo and Dong-Choon Lee

Dept. of Electrical Engineering, Yeungnam University
214-1 Daedong, Gyeongsan, Gyeongbuk, Korea 712-749

Abstract

This paper presents a survey of floating power supply based on bootstrap operation for three-level voltage-source inverters. The floating power supply for upper switches is achieved by the bootstrap capacitor charged during on-time of the switch underneath. Hence, a large number of bulky isolated DC/DC power supplies for each gate driver are reduced. The Pspice simulation results show the behavior of bootstrap devices and the performance of bootstrap capacitor voltage.

Keywords: bootstrap capacitor, floating power supply, gate driver, isolated DC/DC power supply, three-level inverter.

1. Introduction

Neutral-Point-Clamped (NPC) multilevel inverters have been popular in modern drive systems, especially in the integration of renewable energy sources to the utility grid. They can offer better output voltage quality than two-level inverters and reduce the switch voltage rating [1]. However, as the number of level increases, more complicated drive circuits are needed for each switch in an effort to change the state of power semiconductors. Moreover, isolated DC voltage sources required for each gate driver cause an expensive and bulky configuration. To overcome these drawbacks, this paper focuses on studying bootstrap technique to form the capacitors as the floating supplies for each gate driver. The result of this method is that a single DC voltage source could supply the power for all gate drive circuits.

2. Bootstrap Operation

The bootstrap supply is formed by a diode and a capacitor connected as shown in Fig. 1. When the low-side switch, Q_2, is on and the high-side switch, Q_1, is off, the negative terminal of the bootstrap capacitor, C_B, is pulled down to ground leading to the current path flowing from DC voltage source, V_G, through diode, D_B, for charging the capacitor. Otherwise, when Q_1 is on, C_B is disconnected from V_G and operates as a floating supply for high-side driver (HSD) controlling its switch.

This simple and low-cost technique has been widely used as a floating supply for high-side gate drive circuitry of the high-voltage gate-drive IC for many years in two-level inverters. The typical commercial gate drivers are IR21xx family which has the floating channel used to drive IGBTs in the high-side configuration operating up to 600 volts.

However, a bootstrap application in multilevel inverters is still a challenge [2]-[4]. This paper extends their use to three-phase three-level NPC inverter.

Fig. 2 shows the topology of a NPC inverter leg with bootstrap circuit. The details of charging strategy are explained as following sequence. When Q_4 is on, the DC voltage source, V_G, is used to feed directly the gate driver corresponding to IGBT Q_4 and simultaneously charges the capacitor C_{B3} via diode D_3 and resistor R_3. Hence, C_{B3} becomes the floating supply of gate-drive circuitry triggering Q_3.

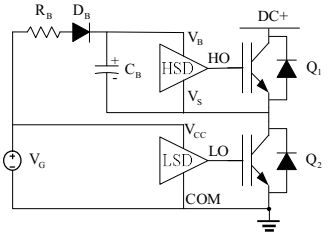

Fig. 1. Bootstrap supply circuit of a two-level inverter leg.

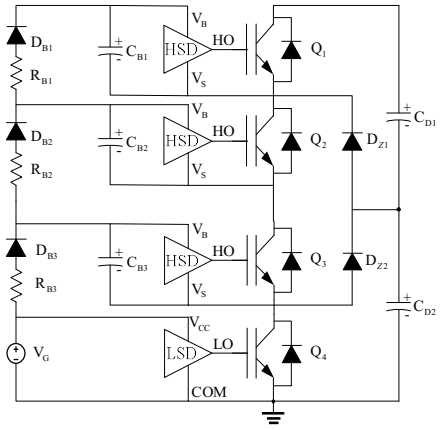

Fig. 2. A three-level NPC voltage source inverter leg.

Similarly, C_{B2} and C_{B1} are used to form the floating supply to drive the IGBTs Q_2 and Q_1, respectively. As a consequence of this operation, C_{B3} and C_{B2} are not only the supplies for their corresponding gate driver of Q_3 and Q_2, but also the supply for charging their upper floating supply.

3. Pulse Width Modulation Control Method

The level-shifted carrier based modulation is applied to the control scheme of NPC inverter. Table I shows the operating status of the switches in the NPC inverter and the correlation between the switching states [1] and the charging of bootstrap capacitors.

TABLE 1
SWITCHING STATES, OUTPUT VOLTAGE AND CHARGED BOOTSTRAP SUPPLY

Switching states	Device switching status (Phase A) $Q_1Q_2Q_3Q_4$	Inverter terminal voltage V_{AZ}	Bootstrap operation
N	0011	-E	C_{B3} is charged by V_G C_{B2} is charged by C_{B3}
O	0110	0	C_{B1} is charged by C_{B2} C_{B2} is charged by C_{B3}
P	1100	E	C_{B1} is charged by C_{B2}

Switching state 'N' denotes that the bottom two switches Q_3 and Q_4 are on and the inverter terminal voltage V_{AZ}, which is the voltage at terminal A with respect to the neutral point Z, is -E. In this case, the DC voltage source V_G directly supplies a power to the gate driver of Q_4 and charges simultaneously to C_{B3}, the floating supply of the gate driver of Q_3, through diode D_3.

Switching state 'O' indicates that the inner two switches Q_2 and Q_3 are on and V_{AZ} is clamped to zero through the clamping diodes. The bootstrap operation is similar: C_{B2} and C_{B1} are charged by C_{B3} and C_{B2}, respectively.

Switching state 'P' indicates that the upper two switches conduct, leading to VAZ=+E. C_{B2} is the power source to both its gate driver and charging the top capacitor C_{B1}.

When a floating supply feeds its gate driver to switch an IGBT and power to upper circuitry, the charge in capacitor is decreased. Hence, the size of the capacitor should be large enough to discharge slowly. This maintains a minimum gate emitter voltage level of bootstrap capacitor in order to remain the switch in conduction without being charged from lower source. The bigger voltage drop on the bootstrap capacitors may cause the IGBTs to operate in linear region and overheat quickly. Moreover, as mentioned earlier, the bootstrap capacitor will be periodically recharged by the lower floating supply in the PWM control scheme of the NPC inverter which results in increasing the amount of the charge. So, the capacitors have to be small enough to charge quickly to obtain the sufficient voltage in the high frequency operation. Furthermore, the forward voltage of semiconductor devices and the total gate charge of IGBTs have to be taken into account when sizing the bootstrap capacitors [4].

In addition, the diode, D_B, plays an important role in minimizing the amount of charge flowing back from capacitor into DC source and its series resistor is placed to limit the initially charged current of bootstrap capacitor. They should be ultra-fast recovery time type with the breakdown voltage larger than DC link voltage [4].

4. Simulation Results

To verify the feasibility of this method, ORCAD/PSPICE simulations have been performed for a three-phase three-level NPC inverter connecting to a DC-link voltage rated at 500V to control RL load.

Fig. 3(a) shows the level-shifted three-level PWM technique where the amplitude modulation index equals to 1, the frequency of reference signal and triangle carrier is set to 50Hz and 5kHz, respectively. Fig. 3(b) shows the load phase-A voltage and Fig. 3(c) shows the load phase-A current. Fig 3(d), (e) and (f) show the bootstrap capacitor voltages of C_{B1}, C_{B2} and C_{B3}, respectively. As can be seen, the obvious reduction in amplitude of the capacitor voltage is from approx 14V for the Q_3 to approx 12V for the top switch, Q_1. However, these voltage values are still larger than the minimum gate emitter voltage which is necessary to drive the IGBTs.

The detail of switching behaviors of the inverter is illustrated in Fig. 4. Fig. 4(a) shows response to the input of gate driver to generate the output which is used to control the state of IGBT. Fig. 4(b) shows the collector-to-emitter voltage of associate IGBT.

5. Conclusion

In this paper, the bootstrap technique applied to a three-level NPC inverter has been presented. This can eliminate the need for individual power transformer for each of the gate driver supplies which require only a single power supply for all the gate drivers. Thus, this method is able to significantly reduce the cost and the size of the three-level inverter.

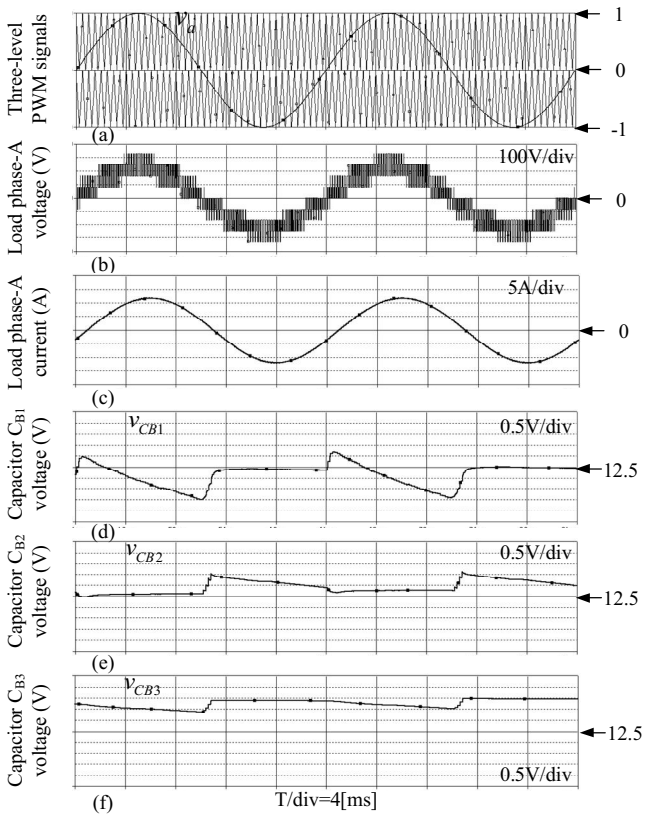

Fig. 3. (a) Three-level carrier based PWM , (b) load phase-A voltage, (c) load phase-A current, (d) bootstrap capacitor C_{B1} voltage, (e) bootstrap capacitor C_{B2} voltage, (f) bootstrap capacitor C_{B3} voltage.

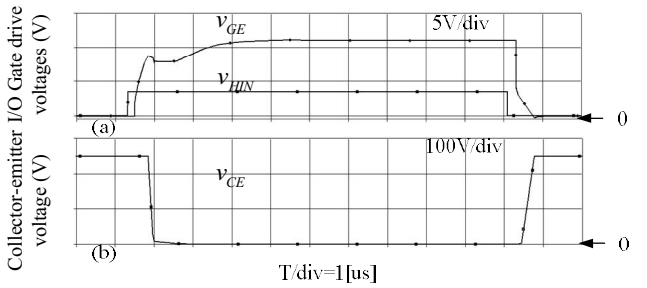

Fig. 4. Switching behavior. (a) Gate driver input and output signals, (b) Collector-to-emitter voltage.

References

[1] Bin Wu, High-power converters and AC drives, Wiley-Interscience, Chapter. 8, 2006.

[2] J. J. Graczkowski, K. L. Neff, and X. Kou, "A low-cost gate driver design using bootstrap capacitors for multilevel MOSFET inverters," in Proc. 5th CES/IEEE Int. Power Electron. Motion Control Conf., Aug. 2006, vol. 2, pp. 1–5.

[3] Felipe J. C. Padilha, Walter Issamu Suemitsu, Maria Dias Bellar and Plutarcho Maravilha Lourenco, "Low-cost gate drive circuit for three-level neutral-point-clamped voltage-source inverter," in IEEE Trans. on Ind. Electron., vol. 56, no. 4, pp. 1196-1204, April 2009.

[4] "Design Tips DT 98-2A," Bootstrap component selection for control. [Online]. Available: http://www.irf.com/technical-info/designtp/ dt98-2.pdf.