Minimization of DC-Link Capacitance for NPC Three-level PWM Converters

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Abstract

This paper presents a control algorithm that minimizes the DC-link capacitance by decreasing the capacitor current. The capacitor current can be nullified by a feedback compensation term which is calculated from the power balance in the AC/DC converter. As a result, voltage variation in the DC-link is reduced further, which makes a large reduction in the size of DC-link capacitors which are expensive and have limitations in life time. Simulations are performed with two 80uF DC-link capacitors, which can be replaced by film capacitors.

1. Introduction

Recently, a great attention has been paid to the three-level neutral-point-clamped voltage source PWM inverter (NPC-VSI) [1]. Further reduction in size, weight and cost of passive components, since the first group of harmonics is centered on twice the switching frequency, is the advantages of these converters over the conventional two-level converters. In order to make a decoupling between the inverter and the converter, the large size of electrolytic capacitors is needed. However, the DC-link capacitor is the critical component in determining the life time of converters. Besides, the DC-link capacitor is bulky, heavy, and expensive. So, it is much desirable to reduce the capacitance size. The minimizing schemes of the DC-link capacitor have been proposed in the conventional two-level converters in [2] - [4]. In this paper, a control algorithm for reducing the DC-link capacitor in three-level NPC converters is presented. The basic idea is to minimize the capacitor current so that the DC-link voltage does not vary much even with smaller capacitance value.

2. System modeling

A per-phase equivalent circuit of the NPC three-level back-to-back converter system is shown in Fig. 1. The e_a, e_b and e_c are the source voltages and L denotes the line inductance. The i_{dc1}, i_{dc2} and i_c represent the currents from the converter to the DC-link, the current from the DC-link to the inverter and capacitor current, respectively. The dynamics of voltages and current can be found by writing the voltage equation of grid-side converter and the DC-link capacitor current equation respectively. To distinguish the converter and inverter variables, subscripts 1 and 2 are selected for converter and inverter respectively. The dynamics of the grid-side converter currents are:

$$e_{de1} = L\frac{di_{de1}}{dt} - \omega L i_{qe1} + v_{de1} \tag{1}$$

$$e_{qe1} = L\frac{di_{qe1}}{dt} + \omega L i_{de1} + v_{qe1} \tag{2}$$

where e_{de} and e_{qe} are dq-axis source voltages in a synchronous reference frame and ω is angular frequency of the source voltage, respectively. By aligning the q-axis of the synchronous reference frame to the source voltage $e_{de} = 0$. By applying the Kirchhoff's current law to the DC-link terminal, the capacitor current is:

$$i_c = i_{dc1} - i_{dc2} = \frac{P_{Conv} - P_{inv}}{v_{dc}} \tag{3}$$

The converter and inverter powers are:

$$p_{Conv} = \frac{3}{2}(e_{de1}i_{de1} + e_{qe1}i_{qe1}), \quad p_{inv} = \frac{3}{2}(e_{de2}i_{de2} + e_{qe2}i_{qe2}) \tag{4}$$

Substituting (4) into (3),

$$i_c = \frac{3}{2v_{dc}}(e_{qe1}i_{qe1} - e_{de2}i_{de2} - e_{qe2}i_{qe2}) \tag{5}$$

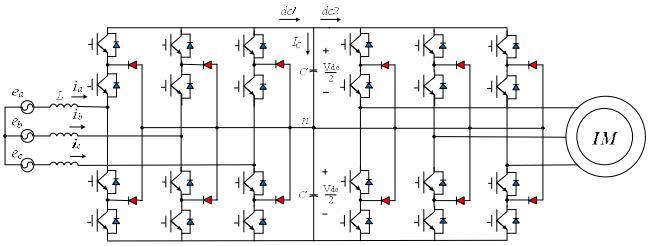

Fig. 1 AC/DC/AC PWM NPC three-level converter.

3. Proposed converter control method

The DC-link voltage is charged by the capacitor current. If the capacitor current is minimized or regulated to zero, then the DC-link voltage does not vary. So, the aim is to minimize the capacitor current. Normally, in converter current controller, the converter-side DC current is used to regulate the DC-link voltage and the inverter-side DC current is utilized as a disturbance. Fig. 2 shows the control algorithm method for capacitor minimization. The effect of capacitor current is fed-back to the output of voltage controller and the new current reference is yielded. So, the capacitor current will be minimized and the capacitor size can be decreased. The feedback part is calculated by the power balance in the converter side and by regulating the d-axis current to zero to achieve unity power factor, the relation of the capacitor current with the grid current, i_{DC}, can be calculated by (6) and (7):

$$i_c = \frac{3}{2v_{dc}}(e_{de1}i_{qe1} + e_{de1}i_{qe1}) = \frac{3}{2v_{dc}}(e_{qe1}i_{qe1}) \tag{6}$$

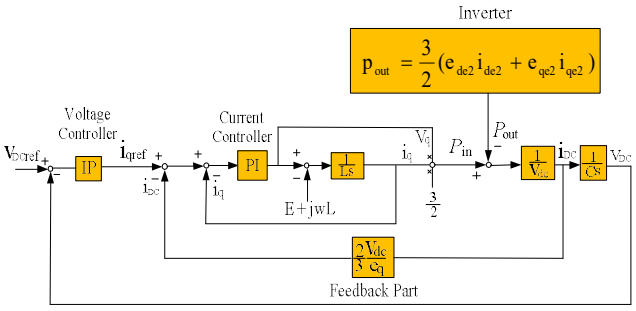

Fig. 2 Block diagram of the proposed controller.

$$i_{DC} = \frac{2v_{dc}}{3e_{qe1}} i_c \tag{7}$$

So, the new q-axis current reference is calculated as:

$$i_{qref1} = i_{qref} - i_{DC} \tag{8}$$

Finally, the outputs of the dq-axis current controller can be expressed in (9) and (10), respectively, in which the anti-windup function is included,

$$v_{d1}^* = -k_p(i_{d1}^* - i_{d1}) + k_i \int ((i_{d1}^* - i_{d1}) + \frac{1}{k_p}(v_{d1}^* - v_{d1}))dt + E_{d1} - L\omega i_{q1} \tag{9}$$

$$v_{q1}^* = -k_p((i_{q1}^* - i_{DC}) - i_{q1}) + k_i \int (((i_{q1}^* - i_{DC}) - i_{q1}) + \frac{1}{k_p}(v_{q1}^* - v_{q1}))dt + E_{q1} + L\omega i_{d1} \tag{10}$$

The gains of the current controller is calculated from the transfer function between the real and reference converter current and the gains of the voltage controller are calculated from the power balance between input and output of converter and by some manual tunings.

4. Simulation results

Simulation was performed under the following environments. The induction machine is 4-pole, 9kW with the stator, mutual and rotor inductances being equal to 59.3(mH), 56.64(mH) and 60.4(mH), respectively. Stator and rotor resistances are 0.39(Ω) and 0.35(Ω). The grid line-to-line voltage is chosen as 380(Vrms)/60Hz, and DC-link voltage, DC-link capacitors, boost inductor, and switching frequency are chosen as 600(V), 80(μF), 0.6(mH) and 5(kHz), respectively.

Fig. 3 shows the simulation results when the speed changes in a stepwise from -1000(rpm) to +1000(rpm). The inverter q-axis current rises up to 40(A), and in the reverse condition when the speed decreases at the same rate, the inverter q-axis current decreases up to -40(A). The converter q-axis current rises up to 15(A). At the time of 0.8(s), a full load condition is applied to the motor and then the inverter q-axis current increased. During this duration, the DC-link voltage variation is kept within 10%.

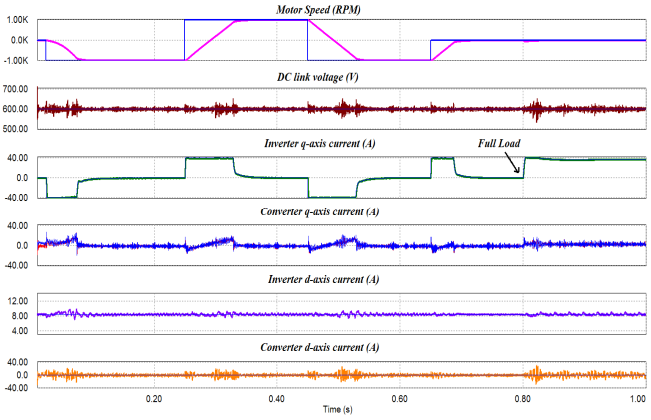

Fig. 3 Simulation results with $C_{1,2} = 80\mu F$ when the motor speed step change from -1000rpm to 1000rpm, with full load applied at 0.8(s).

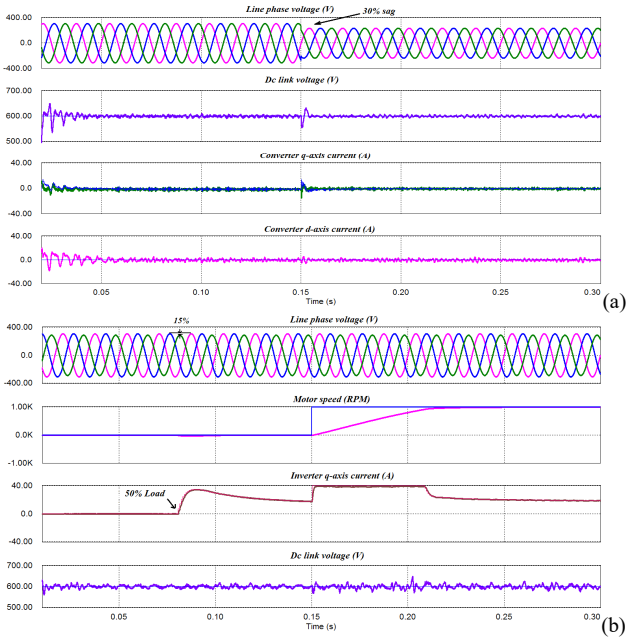

Fig. 4 Simulation results when: (a) Source voltage sag (30%) is taken, (b) Unbalance condition with one phase voltage 15% below the nominal voltage.

Fig. 4(a) shows the voltage controller regulates the DC-link voltage at 30% sag of line voltages by increasing the converter current. In Fig. 4(b), a step change in speed from 0 to 1000rpm at a half load condition is applied to system at unbalance condition, however, the voltage fluctuations are acceptable. As expected, the ripple frequency in the DC-link voltage is $120(Hz)$ which is caused by the negative sequence component [5]. However these ripples do not affect the converter current since the magnitude of ripples is lower than $\pm 15(V)$.

5. Conclusion

In this paper, a capacitance minimization control scheme for the NPC three-level converters has been proposed for induction machine drives. By minimizing the DC-link current, the capacitance size can be reduced. The DC-link voltage controller is effectively regulated under a step change of the speed at full load condition. Even at unbalance or sag voltage conditions, the control performance of the DC-link voltage is very satisfactory. So, the large DC-link electrolytic capacitors can be replaced by small-size film capacitors without deterioration of control performance.

References

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