ZVS Center-Tapped Half-Bridge Zeta Converter with Reduced Output Filter Inductor Size

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Abstract

In this paper, a new half-bridge zeta converter employing a center-tapped rectifier is proposed. The proposed converter provides a bidirectional powering path in the rectifier. As a result, its improved rectifier voltage waveform reduces the output filter inductor size. Also, it maintains a wide ZVS range due to the characteristic of the conventional single-ended half-bridge zeta converter. The operational principles, the theoretical analysis, and the design considerations of the proposed converter are analyzed. To verify the performance of the proposed converter, experimental results from a 180W prototype are presented.

1. Introduction

To minimize the size and weight of the converters, a high switching frequency is generally required. However, the hard switching of the power switch causes the high switching losses. As a result, the various types of the soft switching dc/dc converters have been highlighted for decades. Among them, the conventional single-ended half-bride zeta (SHBZ) converter, which is derived from the zeta converter, is one of the most attractive half-bridge type converters due to a wide ZVS range, the reasonable number of components, and clamping voltage stresses on the primary switches to the input voltage level [1]. However, it features a single-ended type converter, as shown in Fig. 1. That is, while Q_1 only turns on, the power is transferred from the primary side to the output. Therefore, it results in the increase of the output filter inductor size.

To solve the aforementioned drawback of the conventional SHBZ converter caused by single-ended rectifier (SER), this paper proposes the center-tapped half-bridge zeta converter. By adopting the center-tapped rectifier (CTR) to provide the bidirectional powering path, the proposed converter can reduce the output filter inductor size while maintaining the characteristics of the conventional SHBZ converter.

2. The Proposed Converter

2.1 Operational Principle

Fig. 2 and 3 show the circuit diagram and key waveforms of the proposed converter, respectively. The proposed circuit consists of one blocking capacitor (C_B), two primary switches (Q_1, Q_2), one center-tapped transformer (T_1), one rectifier diode (D_s), one link capacitor (C_s), one output filter inductor (L_o), and one output filter capacitor (C_o).

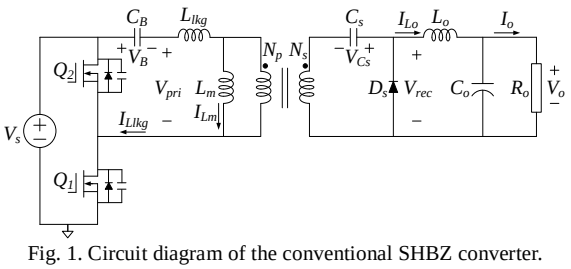


Fig. 1. Circuit diagram of the conventional SHBZ converter.

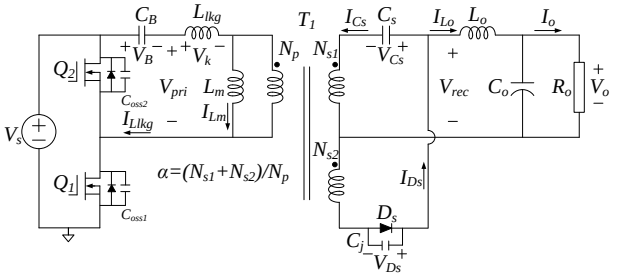


Fig. 2. Circuit diagram of the proposed converter.

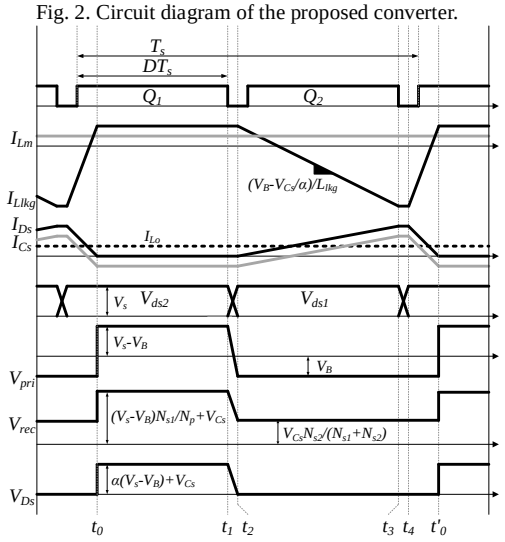


Fig. 3. Key waveforms of the proposed converter.

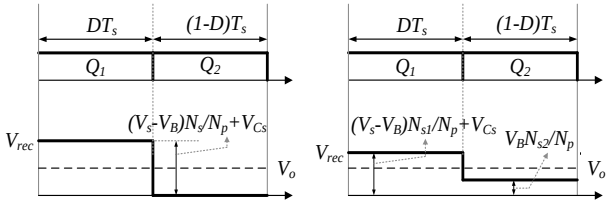
Mode 1[$t_0 - t_1$] : When D_s is turned off at t_0, mode 1 begins. The power is transferred to the output only through C_s. V_s-V_B is applied to the primary side of the transformer and (V_s-V_B)N_{s1}/N_p+V_{Cs} is applied to the output LC filter.

Mode 2[$t_1 - t_2$] : After Q_1 is turned off at t_1, the power is still transferred to the output only through C_s. Therefore, C_{oss1} is charged to V_s and C_{oss2} is discharged to 0 by the reflected load current. Since the ZVS of Q_2 is accomplished by the reflected load current, the ZVS of Q_2 is easily achieved.

Mode 3[$t_2 - t_3$] : At time t_2, V_{ds2} reaches zero and the anti-parallel diode of the switch (Q_2) begins to conduct. It is noted that the CTR provides the powering path from the primary to the output through D_s. Therefore, $V_{rec}=V_{Cs}N_{s2}/(N_{s1}+N_{s2})$, and V_B-V_{Cs}/α is applied across L_{lkg}. As a result, I_{Llkg} decreases and reaches the negative maximum peak current as shown in Fig. 3.

Mode 4[$t_3 - t_4$] : At time t_3, the switch (Q_2) is turned off, and L_{lkg} and $2C_{oss}$ begin to resonate. The energy stored in L_{lkg} charges C_{oss2} to V_s and discharges C_{oss1} to 0. If the energy stored in L_{lkg} is large enough, the ZVS of Q_1 is easily achieved.

Mode 5[$t_4 - t'_0$] : At time t_4, $V_{ds1}(t)$ reaches zero and the anti-parallel diode of the switch (Q_1) begins to conduct. The CTR still provides the powering path from the primary to the output through



(a) Conventional SHBZ converter. (b) Proposed converter.

Fig. 4. Rectifier voltage waveforms.

D_s. Therefore, V_{rec} still maintains $V_{Cs}N_{s2}/(N_{s1}+N_{s2})$, and $V_s+V_{Cs}/\alpha-V_B$ is applied across L_{llkg}. As a result, I_{Llkg} increases as shown in Fig. 3.

2.2 Analysis of the Proposed Converter

2.1.1 DC Conversion Ratio

The voltage-second balance across L_m and L_o can be respectively expressed as follows:

$$(V_s - V_B)DT_s = \frac{V_{Cs}}{\alpha}(1-D)T_s \tag{1}$$

$$\left[(V_s - V_B)\frac{N_{s1}}{N_p} + V_{Cs} - V_o\right]DT_s = \left[V_o - V_{Cs}\frac{N_{s2}}{N_{s1}+N_{s2}}\right](1-D)T_s \tag{2}$$

From mode 3, the following equation can be obtained.

$$\frac{V_k}{L_{llkg}}(1-D)T_s = \frac{2\alpha I_o}{(1-D)} \tag{3}$$

By using (1) - (3), the dc conversion ratio can be expressed as follows:

$$\frac{V_o}{V_s} = \frac{\alpha D}{1+\alpha^2\frac{2D}{(1-D)^2}Q}, \quad \alpha = \frac{N_{s1}+N_{s2}}{N_p}, \quad Q = \frac{L_{llkg}}{T_sR_o} \tag{4}$$

If Q is small enough, the dc conversion ratio can be approximated as follows:

$$\frac{V_o}{V_s} = \alpha D \tag{5}$$

Since the dc conversion ratio of the SHBZ converter is approximately DN_s/N_p, N_s should be the same as $N_{s1}+N_{s2}$ to operate both converters with the same duty.

2.1.2 ZVS Conditions

The ZVS of the switch (Q_1) is achieved by the energy stored in L_{llkg} as mentioned in mode 4. Therefore, The ZVS conditions of the switch (Q_1) can be expressed as follows:

$$\frac{1}{2}\cdot L_{llkg}\cdot\left[\frac{\alpha(1+D)I_o}{(1-D)}\right]^2 \geq 2\cdot\frac{1}{2}\cdot C_{oss}\cdot V_s^2 \tag{6}$$

Since the negative maximum peak value of $I_{Llkg}(t_3)$ is large as shown in Fig. 3, the ZVS range of the switch (Q_1) is wide.

The ZVS of the switch (Q_2) is easily achieved since the ZVS of the switch (Q_2) is accomplished by the reflected load current. The ZVS conditions of switch (Q_2) can be expressed as follows:

$$\frac{1}{2}\cdot L_o\cdot I_o^2 + \frac{1}{2}\cdot L_m\cdot I_{Lm}^2 \geq 2\cdot\frac{1}{2}\cdot C_{oss}\cdot V_s^2 \tag{7}$$

2.1.3 Output Filter

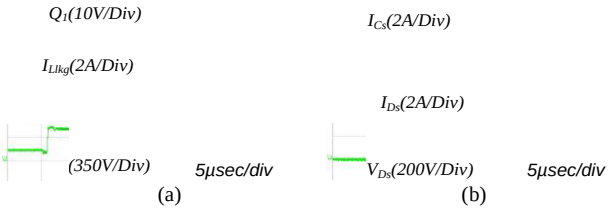
Fig. 4 shows the comparative waveforms of the rectifier voltage (V_{rec}) of the SHBZ converter and the proposed converter. As can be seen in this figure, the ac content of V_{rec} is much smaller in the proposed converter compared with the SHBZ converter.

The peak-to-peak output inductor current ripples of the SHBZ converter and the proposed converter are respectively calculated from the voltage-second balance on L_o as follows:

$$\Delta i_{Lo\_SHBZ} = \frac{V_o(1-D)T_s}{L_o} \tag{8}$$

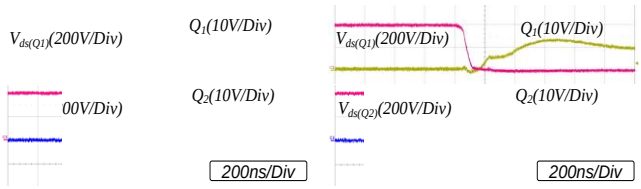
$$\Delta i_{Lo\_Proposed} = \frac{1}{L_o}\cdot(V_o - \frac{N_{s2}}{N_p}\cdot V_B)\cdot(1-D)\cdot T_s \tag{9}$$

Therefore, the proposed converter can employ smaller output



(a) (b)

Fig. 5. Experimental waveforms for nominal input voltage at a full load. (a) Q_1, I_{Llkg}, and V_{rec}. (b) I_{Cs}, I_{Ds}, and V_{Ds}.



(a) (b)

Fig. 6. ZVS waveforms (Q_1, Q_2). (a) at full load conditions. (b) at 40% load conditions.

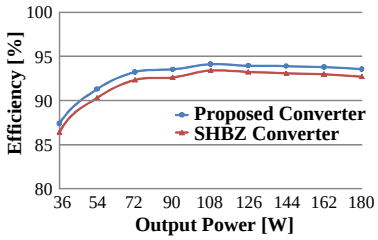


Fig. 7. Measured efficiency.

filter inductor than the SHBZ converter.

3. Experimental Results

The prototype of the proposed converter has been built and tested with specifications as follows:

- V_s=300~400V, V_o=200V, I_o=0.9A, f_s=65kHz
- C_B=C_s=2.2μF, C_o=225nF
- L_m=2mH, L_{llkg}=40μH, L_o=1.3mH, N_p:N_{s1}: N_{s2}=50:27:34
- Q_1=Q_2=FCPF16N60, D_s=RHRP1560

To remove the voltage ringing across the rectifier diode of the secondary side of the proposed converter, the RCD snubber circuit is adopted with the following specifications: R_{snb}=14kΩ, C_{snb}=10nF, D_{snb}=UF4004.

Fig. 5 shows that all waveforms are well agreed with the theoretical analysis.

Fig. 6 shows the ZVS waveforms of Q_1 and Q_2 at 40% and full load conditions. It is noted that the ZVS of Q_2 is easily achieved by the reflected load current at 40% load conditions, and the ZVS of Q_1 is achieved at 40% load conditions by the energy stored in L_{llkg}.

Fig. 7 shows the measured efficiency curves of the SHBZ converter and the proposed converter according to the load variation. The reduced output filter inductor size contributes to the efficiency improvement.

4. Conclusion

A center-tapped half-bridge zeta converter, which has a bidirectional powering path in the rectifier, is proposed. Its improved rectifier voltage waveform reduces the output filter inductor size while maintaining the characteristics of the conventional single-ended half-bridge zeta converter.

Reference

[1] T. F. Wu, S. A. Liang, and Y. M. Chen, "Design optimization for asymmetrical ZVS-PWM Zeta converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 2, pp. 521-532, Apr. 2003.