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Thermal Stability of Self-formed Barrier Stability Using Cu-V Thin Films

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Recently, scaling down of ULSI (Ultra Large Scale Integration) circuit of CMOS (Complementary Meta Oxide Semiconductor) based electronic devices, the electronic devices, become much faster and smaller size that are promising property of semiconductor market. However, very narrow interconnect line width has some disadvantages. Deposition of conformal and thin barrier is not easy. And metallization process needs deposition of diffusion barrier and glue layer for EP/ELP deposition. Thus, there is not enough space for copper filling process. In order to get over these negative effects, simple process of copper metallization is important.

In this study, Cu-V alloy layer was deposited using of DC/RF magnetron sputter deposition system. Cu-V alloy film was deposited on the plane SiO2/Si bi-layer substrate with smooth surface. Cu-V film's thickness was about 50 nm. Cu-V alloy film deposited at 150°C. XRD, AFM, Hall measurement system, and AES were used to analyze this work. For the barrier formation, annealing temperature was 300, 400, 500°C (1 hour). Barrier thermal stability was tested by I-V(leakage current) and XRD analysis after 300, 500, 700°C (12 hour) annealing.

With this research, over 500°C annealed barrier has large leakage current. However vanadium-based diffusion barrier annealed at 400°C has good thermal stability. Therefore thermal stability of vanadium-based diffusion barrier is desirable for copper interconnection.

Keywords: Copper interconnect, Diffusion barrier, DC/RF magnetron sputter, Thermal stability, Self-formed barrier