Information Technology System-on-Chip

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ABSTRACT

This paper presented a method constructing the ITSoC(Information Technology System-on-Chip). In order to implement the ITSoC, designers are increasing relying on reuse of intellectual property(IP) blocks. Since IP blocks are pre-designed and pre-verified, the designer can concentrate on the complete system without having to worry about the correctness or performance of the individual components. Also, embedded core in an ITSoC access mechanisms are required to test them at the system level. That is the goal, in theory. In practice, assembling an ITSoC using IP blocks is still an error-prone, labor-intensive and time-consuming process. This paper discuss the main challenge in ITSoC designs using IP blocks and elaborates on the methodology and tools being put in place for addressing the problem. It explains ITSoC architecture and gives algorithmic details on the high-level tools being developed for ITSoC design.

요 약

본 논문에서는 정보기술 시스템온칩을 구성하는 방법을 제안하였다. 시스템온칩을 구현하기 위해 설계자는 IP의 재사용을 염두해 두어야 한다. IP 블록은 미리 설계되어지고 검증되기 때문에 설계자는 개별 부품의 올바름과 수행에 대해 거정을 하지 않아도 된다.또한, 정보기술 시스템온침의 임베디드된 코어는 시스템 레벨의 테스트 메카니즘을 호출하여 사용한다. 실제에 있어, IP 블록을 사용하여 조립할 때 아직까지는 error-prone, labor-intensive, time-consuming 과정을 사용한다. 본 논문에서는 시스템온칩 설계자가 IP 블록과 툴을 사용하는 것에 촛점을 맞추었다.

키워드

Information Technology, System-on Chip, IP block

Ⅰ. Introduction

Embedded system[1-4] are now widespread in large information technology system-on-a-chip(ITSoC)[5] designs]. However, since embedded cores not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. The design of the test access architecture is especially important for the system designer/integrator, which is being developed for embedded core testing. A test access architecture, also referred to as a test access mechanism, provides means for on-chip test data transport. It can be used to transport test patterns from a pattern source to a core-under-test, and transport test responses from a core-under-test to a response monitor. A number of test access architectures have been proposed in the literature[6]. In order to reduce test cost, the testing time for a core-based system should be minimized by adopting an

appropriate test access architecture. Today's market reality in VLSI design is characterized by : short time-to-market, large time-to-market is paramount, complexity and performance cannot be compromised, at the risk of reaching the market with an uncompetitive product. This demanding environment is forcing fundamental changes in the way VLSI systems are designed. The use of pre0designed IP blocks(henceforth called cores) for SoC design has become essential in order to build the required complexity in a short time-to-market.

Ⅱ. ITSoC Target Architecture

In the early stages of ITSoC design, cores were designed with many different interfaces and communication protocols. In order to avoid this problem, standards for on-chip bus structures were developed. Currently there are a few publicy available bus architectures from leading manufactures. These bus architectures are usually tied to a processors architecture, such as PowerPC or the ARM. The cores provided by these manufactures are optimized to work with such bus architectures, thus requiring minimal extra interface logic. The cores are predesigned and preverified to work with the Connect bus architecture and protocols, thus allowing for reuse from chip to chip. Fig. 1 illustrates a connect-based ITSoC. Although the cores are designed to interface with the buses almost directly, the designer still has connect hundreds of pins and define the parameters for all cores.

Ⅲ. Interconnection Engine

Properties are used for establishing correspondence between a virtual pin and the real pins with similar functionality, as well as for matching up real pins in different components. By comparing properties on pins the tool can decide whether the functionality of as real pin falls within the functionality of a virtual pin. Since the complete ITSoC may have hundreds to thousands of internal pins, these comparisons need to done very efficiently and in a general manner. Moreover, the algorithm needs to be able to handle not only exact matches but also overlapping sets(not exact match).

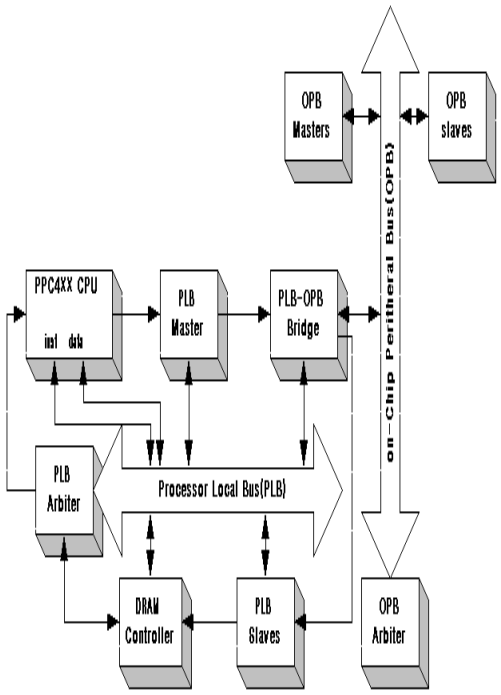

Fig.1. ITSoC using the CoreConnect bus architecture

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