Capacitive Sensing Circuit for Low Power and High Resolution

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ABSTRACT

This paper describes the possibility of a low-power, high-resolution fingerprint sensor chip. A modified capacitive detection circuit of charge sharing scheme is proposed, which reduces the static power dissipation and increases the voltage difference between a ridge and valley more than conventional circuit. The detection circuit is designed and simulated in 3.3V, 0.35㎛ standard CMOS process, 40MHz condition. The result shows about 35% power dissipation reduction and 90% improvement of difference between a ridge and valley sensing voltage. The proposed circuit is more stable and effective than a typical circuit.

KEYWORD

capacitive sensing, detection circuit, low power, high resolution, CMOS, VLSI

Ⅰ. INTRODUCTION

A fingerprint is made of a series of ridges and valleys on the surface of the finger. In a capacitive fingerprint sensor, the finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of a silicon chip and air. By measuring the variances of the capacitance according to the distance from the chip surface to the finger's skin, the pattern of a fingerprint, i.e. ridges and valleys, can be obtained. A capacitive fingerprint sensor uses a capacitive sensor array to detect fingerprints.

One of the most important performances of a capacitive sensor is the sensitivity capability since the capacitance to be detected is very small of the order of femtofarads. A charge-sharing sensing scheme has a high sensitivity and a simple circuit structure for the restricted pixel area below a sensor plate. Some papers on charge-sharing sensing scheme have been published [1-3]. The paper [1] proposed the removing of parasitic capacitance using unit-gain buffer, and paper [2-3] proposed the improvement of difference between a ridge and valley detection voltage using a feedback resistor. Although these methods above are useful in dramatic performance improvement, a static current can exist on a sensing enable phase in these circuits because of a unit-gain buffer and feedback resistor. This paper proposes a modified circuit for reduction of the static power dissipation and increasing the voltage difference between a ridge and valley more than conventional circuit.

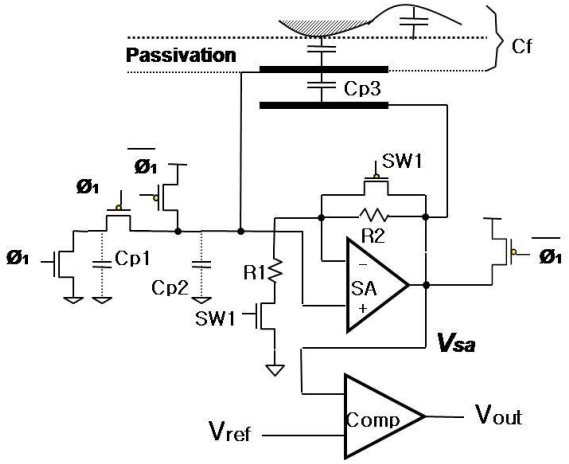
Ⅱ. Capacitive sensing scheme

Fig. 1 shows a conventional capacitive charge-sharing sensing scheme and timing

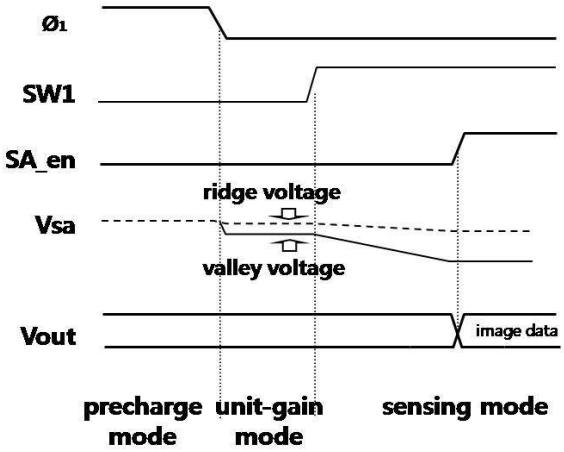
diagram[3]. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of the silicon chip and air. The series-connected capacitor Cf is composed of a capacitor between the metal plate and the chip surface and another one between the chip surface and the finger skin. The capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. The variation of capacitance is transferred to output voltage by sensing scheme. The comparator discriminates a ridge and valley by reference voltage, Vref.

In Fig. 1, "SA" is a unit-gain buffer and "Comp" is a comparator. In the precharge phase, no charge is accumulated in Cp3 because the two electrodes have the same potential. In Cp2 and Cf, the amount of charge stored is Cp2 VDD and Cf VDD. At the beginning of the unit-gain phase, the charges stored in the precharge are redistributed between the nodes. The SA tracks the voltage change of the node Vsa, which makes the potential difference between the two electrodes of Cp3 zero. Therefore, It can remove the influence of Cp3. In the sensing phase, SW1 is high and SA operates as an attenuator by R1 and R2 ratio. Through the simulation which is repeated, R1 is 5k and R2 is 1.4 k. The comparator 'Comp' is enabled by the signal 'SA_en' and compares the voltage of Vsa with the external reference voltage Vref. Thus, a binary output according to the finger pattern is produced. SA operates as an attenuator, as well as a unit-gain buffer by handling the switching signal, SW1.

The operation and power consumption can be seen by the HSPICE simulation of the cell on condition of 40MHz, 0.35m typical parameter and 3.3V power supply in Fig. 2. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) is 1720mV



(a) Sensing circuit



(b) Timing diagram

Fig. 1 Conventional capacitive charge-sharing sensing scheme

after sensing phase. Thereby, the comparator easily discriminates the ridge and valley. Even though the voltage difference is increased, there is power consumption by the static current. It is caused by the unit-gain buffer and feedback registers.

In sensing phase, when Vsa of a valley starts to decrease due to feedback registers in sensing phase, the voltage cannot decrease fast enough. Because SA_en enables after Vsa fully discharges to 0 voltage, duration of static current is long.

The average current is 605 uA in a ridge and 204 uA in a valley at 3.3V, 40MHz operation condition. If the occurrence number of a ridge and valley is same, the average current is 404 uA in general operation.

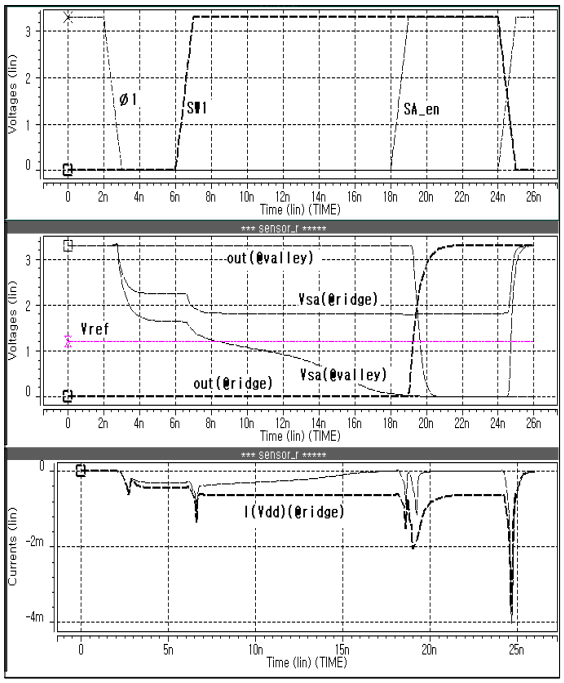
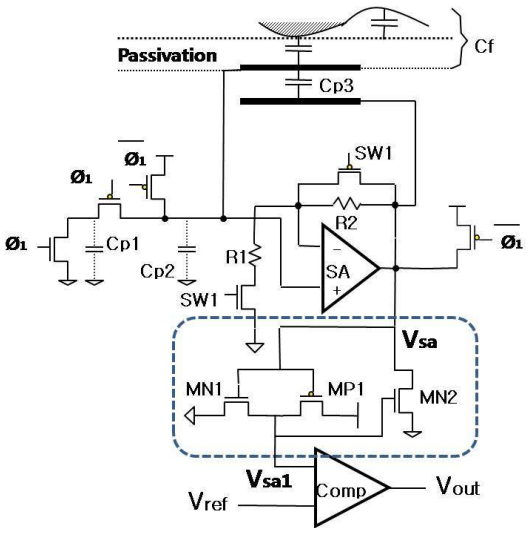


Fig. 2 Simulation result of conventional circuit
(3.3V, 0.35 □m CMOS process typical condition, 40MHz)

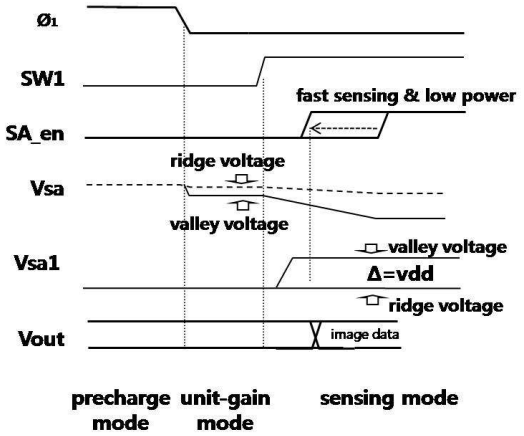
IV. PROPOSED SENSING SCHEME

Fig. 3 shows the proposed capacitive sensing circuit. To accelerate fast sensing of the voltage decrease of Vsa we inserted an inverter with a small size transistor MP1, MN1 into conventional sensing configuration. MN2 is a source follower. The width of MN1 transistor is designed more than MP1. Therefore, the logic threshold voltage of the inverter is less than VDD/2 for fast pull-up of Vsa1 in a valley. As a result, we can make fast SA_en enable time. It means reduction of static current duration. Fig. 4 shows the function and power dissipation result. In a valley, Vsa1 reaches high voltage fast by the inserted inverter without waiting of slow decrease of Vsa. The average current is 385 uA in a ridge and 136 uA in a valley at 3.3V, 40MHz operation condition. If the number of a ridge and valley is same, the average current is 260 uA in general operation. It means 35% reduction of power consumption.

Vsa1 is comparator input voltage. In proposed circuit, because Vsa1 is fully VDD in a valley and about 0 voltage in a ridge, the voltage difference between a ridge and valley is about VDD in sensing phase. Our method produces about 90% improvement in the voltage difference between ridge and valley. As a result, we can get high-quality images without the influence of the reference voltage(Vref) variation according to a pixel location of the sensor array.



(a) Modified Sensing circuit



(b) Timing diagram

Fig. 3 Proposedcapacitive charge-sharing sensing scheme

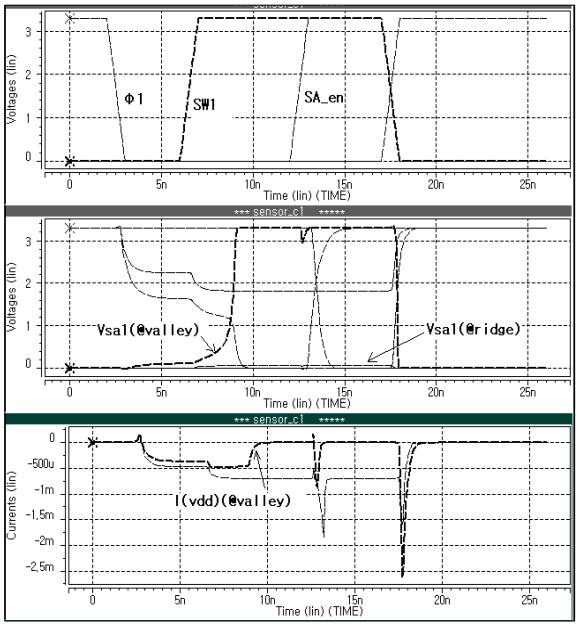


Fig. 4 Simulation result of proposed circuit (3.3V, 0.35 ㎛ CMOS process typical condition, 40MHz)

IV. CONCLUSIONS

This paper proposes a modified hardware scheme of capacitive charge-sharing fingerprint sensors for low power consumption and high image resolution. In the conventional circuit, even though the voltage difference is increased, there is power consumption by the static current. The average current was 404 uA in general operation.

The modified capacitive detection circuit of charge sharing scheme includes an inverter and source follower with a small size transistor to accelerate fast sensing of comparator. The logic threshold voltage of the inverter is less than VDD/2 for fast pull-up of a valley sensing voltage. As a result, we can make fast comparator enable time. It means reduction of static current duration. In addition, because sensing voltage of a valley is fully VDD and about 0 volt in a ridge, the voltage difference between a ridge and valley is about VDD. The modified detection circuit is designed and simulated in a 0.35 ㎛ standard CMOS process, 40MHz frequency condition. The result is about 35% power dissipation reduction and 90% improvement of difference between a ridge and valley sensing voltage.

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