Low Power Test for SoC(System-On-Chip)

정준모*

*군산대학교

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Jun-mo Jung*

*Kunsan National University

E-mail : jmjung@kunsan.ac.kr

요 약

SoC(System-On-Chip)을 테스트 하는 동안 소모하는 전력소모는 SoC내의 IP 코어가 증가됨에 따라 매우 중요한 요소가 되었다. 본 논문에서는 Scan Latch Reordering과 Clock Gating 기법을 적용하여 scan-in 전력소모를 줄이는 알고리즘을 제안한다. Scan vector들의 해밍거리를 최소로 하는 새로운 Scan Latch Reordering을 적용하였으며 Gated scan 셀을 사용하여 저전력을 구현하였다. ISCAS 89 벤치마크 회로에 적용하여 실험한 결과 모든 회로에 대하여 향상된 전력소모를 보였다.

ABSTRACT

Power consumption during testing System-On-Chip (SOC) are becoming increasingly important as the IP core increases in SOC. We present a new algorithm to reduce the scan-in power using the modified scan latch reordering and clock gating. We apply scan latch reordering technique for minimizing the hamming distance in scan vectors. Also, during scan latch reordering, the don't care inputs in scan vectors are assigned for low power. Also, we apply the clock gated scan cells. Experimental results for ISCAS 89 benchmark circuits show that reduced low power scan testing can be achieved in all cases.

키워드

SoC, low power test, scan circuit

Ⅰ. Introduction

The SoC(System-On-chip) revolution has brought some new challenges to both design and test engineers. among these challenges, the power dissipation is one of the most important issues[1]. In [2], a survey on low power testing is given which classifies the recent techniques into low power external test and low power BIST(Built In Self Test). In this paper, we focus on the scan based design that belongs to the external test category[2].

The power of digital system is considerably higher in test mode than in normal mode. The reason is that test patterns cause as many nodes switching as possible while normal mode only activates a few modules at the same time. Special care must be taken to ensure that the power consumption is not exceeded during test application.

A new ATPG tool[3] was proposed to overcome the low correlation between consecutive test vectors during test application. The methods about low power mapping and test compression for unspecified scan vectors were proposed[4,5]. Also, a new compression and low power consumption technique using Scan Latch Reordering(SLR) was proposed[6,7]. It mapped the don't care input for low power and performed the SLR[8].

This paper presents efficient low power test for sequential circuits with full-scan circuits. We applies the low power mapping and clock gating. The power consumption during scan-in can be

effectively reduced by the method which assigns neighboring input value to don't care inputs during scan latch reordering. The clock power can be minimized using scan cell with clock gating method. Also the new scan latch reordering is applied to minimize the hamming distance between adjacent scan cells.

II. Power Consumption model

1) Power Consumption model

Power dissipation in CMOS circuits can be classified into static, short circuit, leakage and dynamic power dissipation. The static power is negligible. The short circuit power dissipation caused by short circuit current and power dissipated by leakage currents contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs. If the gate is part of a synchronous digital circuit controlled by global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is :

$$P_d = 0.5 C_{load} V_{dd}^2 F_c N_g$$

, where C_{load} is the load capacitance, V_{dd} is the supply voltage, F_c is the global clock frequency, and N_g is the total number of gate output transitions

These transitions are major factor of power dissipation. The power dissipation during full-scan testing is due to the dynamic power by transitions occurred when the scan vectors are shifted in the scan chain.

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2) Scan-in power model

Power consumption in testing a sequential circuit with a single scan chain includes; a scan-in power consumed during the scan-in operations of scan vectors, scan-out power consumed during the scan-out operations of test response and a power consumed in combinational logic of the sequential circuit. It is difficult to estimate the scan-out power directly from the scan vector set since the test response must be determined from the function of the core under test. We consider the scan-in power only and measure it in terms of Weighted Transition Metric (WTM).

The scan-in power depends not only on the number of transitions in it but also on their relative positions. For example, consider the scan vector $S_1S_2S_3S_4S_5$ = 10101 with scan length 5. If the left most bit(S_1) is first shifted in the scan chain, the transition of(S_1,S_2) causes four(scan lengh -1) transitions during scan-in. Therefore, the transition of (S_j, S_{j+1}) causes (scan length - j) transitions.

Let each scan vector SV with scan length k be S_1S_2,,,S_KS. The scan-in power for SV is given by

$$P_{\_SV} = WTM(SV) = \sum_{j=1}^{k-1} (S_j \oplus S_{j+1})(k-j)$$

Also, assuing that the set of scan vector used for testing is SV_set=SV_1SV_2,,SV_n, the power consumed during scan-in of SV_set is ;

$$WTM(SV_{\_set}) = \sum_{i=1}^{n} WTM(SV_i)$$

Therefore, the average power consumption and peak power consumption can be represented such as below.

$$P_{avg} = WTM(SV_{\_set})/n$$

$$P_{peak} = Max(WTM(SV_i))$$

III. Scan Latch Reordering and Clock Gating

1) Cost function for scan latch reordering

Let's denote SV_set be SV[r][c] of two dimensional array, whose number of scan vector is r and input number of scan vector is c. Each element of array, SV[i][j] means the j^{th} scan input of the i^{th} scan vector.

The WTM(SV_set) is described as below.

$$WTM(SV_{\_set}) = \sum_{i=1}^{r}\sum_{j=1}^{c-1} (SV[i][j] \oplus SV[i][j+1])(c-j)$$

$$= \sum_{j=1}^{c-1}\sum_{i=1}^{r} (SV[i][j] \oplus SV[i][j+1])(c-j)$$

$$= \sum_{j=1}^{c-1} HD\_col(j, j+1)(c-j)$$

In above equation, we can define the HD_col(j,j+1) as the hamming distance between j^{th} column and $(j+1)^{th}$ column for all rows. In order for WTM(SV_set) to be small, the HD_col

must be small. the HD_col must be small. The scan latch reordering means the reordering of column position in scan vectors. Therefore, it will be good to use the column hamming distance as the cost function of scan latch reordering.

2) Clock gating

The clock signal is a major source of dynamic power dissipation. The clock gating have become a popular way to reduce the transition in sequential circuit. Also, There are many F/Fs in scan chains. The power consumption during scan −in can be reduced by clock gating in scan cells because the scan cells have the same logic value during scan test.

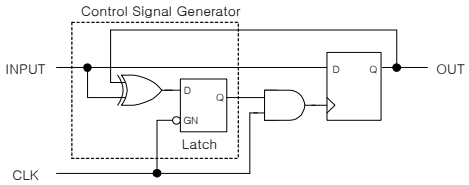

Figure 1. Clock gating

3) Proposed Algorithm

HD_col(j,j+1) is the Hamming Distance of between column j and j+1, and calculate it considering don't care input.

Given SV[i][j] ∈ {0,1,X(don't care input)}, the hamming distance between SV[i][j] and SV[i][j+1] is 1 only in the condition that (SV[i][j], SV[i][j+1]) is (0,1) or (1,0). In case of (0,X) and (1,X), the hamming distance becomes 0 because the value of SV[i][j] can be assigned to X existing in SV[i][j+1].

Because scan latch reordering is a Np−hard problem, it is very difficult to find near optimal solution. We propose Heuristic algorithm below.

· Define SV[*][j] as j^{th}column in two dimensional array of scan vectors.

· Initialize arbitrary SV[*][j] to SV[*][1]. And assign 0 to all X within SV[*][1].

· Choose minimized j after calculating Hamming Distance about SV[*][1] and all SV[*][j]. And exchange SV[*][2] and SV[*][j]. The transition of SV[*][1] and SV[*][2] becomes the minimum.

· By assigning the value of SV[*][2] existing in the same row to X within SV[*][1], prevent the transition from occurring.

In this way, carry out reordering about all SV[*][[j] to make Hamming Distance the minimum.

The proposed algorithm can be described by pseudo code at Figure 2.

```
SV_set = SV[r][c];
Initialize SV[*][1]; /* Initialization of SV[*][1]
                        to arbitrary SV[i][j]. */
For(j=1; j<c; j++)
{
    for(k=j+1; k<c+1;k++)
      HD_col(j,k); /* Calculate  HD_col */

      Search the index k with minimum HD_col;
      Exchange the column j+1 with column k;

}
HD_col(j,k)
{      HD_sum(k) = 0;
        for( i =1; i<r+1; i++)
          if( (SV[i][j] == 0 && SV[i][k]== 1) |
              SV[i][j] == 1 && SV[i][k]== 0) )
                          HD_sum(k)++;
}
Apply Clock gating
```

Figure 2. Proposed Algorithm

IV. Experimental Results

In this section, we evaluate the effect of the proposed method in power consumption during scan testing for ISCAS89 benchmark circuits. The experiments were conducted on a Sum Ultra 10 workstation.

We considered full−scan sequential circuits. For each full−scan circuit, we assumed a single scan chain for our experiments. We used partially−specified scan vector sets generated by MINTEST Automatic Test Pattern Generation (ATPG) program with dynamic compaction [9].

In the column compression ratios, sub column 0 Mapping maps only 0 to don't care inputs [4]. The MTC Map & SLR is the proposed method in [8].

Table 1 shows the reduction ratios for peak power.

The power consumption in our method is reduced to 37% less than MTC Map &SLR in case of s5378. Also, The power consumption in our method is reduced to 73% less than MTC Map &SLR in case of s38417. in our method.

The experimental results show that the proposed method has a better reduction ratio than previous method.

Table 1. Reduction Ratios for Peak Power

Circuit	0 Mapping	MTC Map & SLR	Proposed	
	Peak	Peak	Peak	%
S5378	10127	5556	3464	37
S9234	12994	7400	4798	35
S13207	101127	35486	11327	68
S15850	81832	33207	12131	63
S38417	505295	181436	48631	73
S38584	531321	187379	100319	46

Table 2. Reduction Ratios for Average Power

Circuit	0 Mapping	MTC Map & SLR	Proposed	
	Avg	Avg	Avg	%
S5378	3336	2435	860	65
S9234	5692	3466	1021	70
S13207	12416	7703	766	90
S15850	20742	13381	2162	83
S38417	172665	112198	15960	86
S38584	136634	88298	18235	79

While it is about 5692 in 0 Mapping, 7703 in MTC&SLR in the case of s13207 , the proposed method gives a good result of 766. About power reduction rate, , showed are about 90% less than MTC&SLR in this case.

As showed in above experimental results, the proposed method has higher power reduction ratios.

V. 결 론

As the number of the IP core increases in the SOC, test data volume and testing time increase too. As a result, the testing and chip costs go up and productivity goes down. Also, power consumption in test mode is much larger than that in normal mode and causes damage on chip due to excessive power consumption.

This paper proposes a new algorithm that has efficient low power for unspecified scan vectors. It applies mapping don't care input at the same time of performing scan latch reordering using the hamming distance as the cost function. The proposed method shows extremely power reduction as compared to the previous method.

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