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Electrical characteristics of SiC thin film charge trap memory with barrier engineered tunnel layer

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Recently, nonvolatile memories (NVM) of various types have been researched to improve the electrical performance such as program/erase voltages, speed and retention times. Also, the charge trap memory is a strong candidate to realize the ultra dense 20-nm scale NVM. Furthermore, the high charge efficiency and the thermal stability of SiC nanocrystals NVM with single SiO_2 tunnel barrier have been reported. [1-2]

In this study, the SiC charge trap NVM was fabricated and electrical properties were characterized. The 100-nm thick Poly-Si layer was deposited to confined source/drain region by using low-pressure chemical vapor deposition (LP-CVD). After etching and lithography process for fabricate the gate region, the $Si_3N_4/SiO_2/Si_3N_4$ (NON) and $SiO_2/Si_3N_4/SiO_2$ (ONO) barrier engineered tunnel layer were deposited by using LP-CVD. The equivalent oxide thickness of NON and ONO tunnel layer are 5.2 nm and 5.6 nm, respectively. By using ultra-high vacuum magnetron sputtering with base pressure 3x10-10 Torr, the 2-nm SiC and 20-nm SiO_2 were successively deposited on ONO and NON tunnel layers. Finally, after deposited 200-nm thick Al layer, the source, drain and gate areas were defined by using reactive-ion etching and photolithography. The lengths of squire gate are 2 μm, 5 μm and 10 μm. The electrical properties of devices were measured by using a HP 4156A precision semiconductor parameter analyzer, E4980A LCR capacitor meter and an Agilent 81104A pulse pattern generator system. The electrical characteristics such as the memory effect, program/erase speeds, operation voltages, and retention time of SiC charge trap memory device with barrier engineered tunnel layer will be discussed.

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