A New On-Line Dead-Time Compensator for Single-Phase PV Inverter
단상 PV 인버터용 온-라인 데드타임 보상기 연구

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Abstract

Abstract - This paper presents a new software-based on-line dead-time compensation technique for single-phase grid-connected photovoltaic (PV) inverter system. To improve the mitigation of dead-time effect around the zero-crossing point of phase current, a selective harmonic elimination of instantaneous feedback current is used as an additional part of conventional current control scheme. Simulation and experimental results are shown to verify the effectiveness of proposed compensation method in the grid-connected power distributed generation systems.

1. Introduction

In recent years, the techniques developed for voltage-fed dc/ac Pulse Width Modulation (PWM) inverter has gained wide attention, where the switching devices such as IGBT, MOSFET and others have very high switching frequency above tens of kilohertz are normally used. Since the switching device has a finite switching time, a blank time (dead-time) must be inserted into the PWM gating signals in order to avoid the conduction overlap of two switching devices in the same leg. This dead-time causes the dependent magnitude, phase error, serious output voltage distortions and fundamental voltage drop which degrade the control performance and hence, may cause the power loss during generation process.

In order to overcome these problems caused by dead-time effect, various approaches have been presented. Some of them are the dead-time compensation voltage (DTCV)[1], the dead-time compensation time (DTCT)[2] or modified DTCV[3]. But these methods are not adaptive and cannot compensate the on-voltages effects, or DTCT is not always valid because of varying with the operating points or need a prepared loop-up table.

Fig. 1 Grid current flow and inverter output voltage waveforms ((a) and (b): when $I_g>0$; (c) and (d): when $I_g<0$)

In this paper, a new dead-time compensation strategy for single-phase grid-connected PV inverter based on adaptive noise-canceling algorithm for elimination of single frequency from signal which is used in digital signal processing (DSP). Since the synchronous controllers can be transformed and implemented in a stationary frame of reference preserving their original features from synchronous frame, harmonic components can be selectively eliminated. A selective harmonic elimination dead-time compensator (SHEDC) is introduced as an additional part of current controller and is used to mitigate the 3rd and 5th harmonic components caused by the dead-time effect in generated grid current. Theoretical simulation analysis is carried out and the current control strategy integrated with SHEDC is fully implemented in a 32-bit fixed-point TMS320F2812 DSP for a 3kW single-phase PV inverter experimental prototype with 10kHz switching-frequency and 3µs dead-time.

2. Selective Harmonic Elimination Dead-Time Compensator (SHEDC)

The relationship between ideal and real inverter output voltage is shown in Fig. 1, where Fig. 1(a) shows the grid phase current I_g flow and Fig. 1(b) shows the corresponding inverter output voltage in positive direction ($I_g > 0$). Those of current in negative direction ($I_g < 0$) are shown in Fig. 1(c) and (d).

As shown in Fig. 1(a), the grid current I_g flows through switching device S_1 during the on-switching-period of S_1. Vice versa, I_g flows through diode D_2 during the off-switching-period of S_1 and the dead-time period. It means that the inverter output voltage V_{AN} during off-switching-period of S_1 and during dead-time period has the same characteristics.

The effect of dead-time on inverter output voltage in case direction $I_g > 0$ is shown in Fig. 1(b). Because of dead-time T_d, the real inverter output voltage becomes $V_{AN,DT}$. If the finite turn-on (t_{on}) and turn-off (t_{off}) time of switching device S1 are taken into account, the real voltage becomes $V_{AN,DT,ton/off}$. Furthermore, real inverter output voltage becomes $V_{AN,DT,ton/off,Vs/d}$, if considering the on-voltage V_S dropped on switching device and dropped voltage V_D on the diode D_2. Similarly, the negative direction case has the same analysis as positive case, such as Fig. 1(c) and (d).

To eliminate the unexpected harmonic component from a signal in DSP area, a selective harmonic elimination filter (SHEF) using Least Mean Square (LMS) adaptation algorithm, was introduced in [4][5], is used as illustrated in Fig. 2.

The error ε_k and weight coefficients w_k can be obtained as:

$$\varepsilon_k = d_k - y_k = d_k - \left(x_k^s w_k^s + x_k^c w_k^c \right) \tag{1}$$

$$w_{k+1} = w_k + 2\mu\varepsilon_k x_k \tag{2}$$

where x_k is the harmonic input should be eliminated, d_k is primary signal, y_k is output signal of SHEF, ε_k is the error between d_k and y_k, μ is the adaption gain.
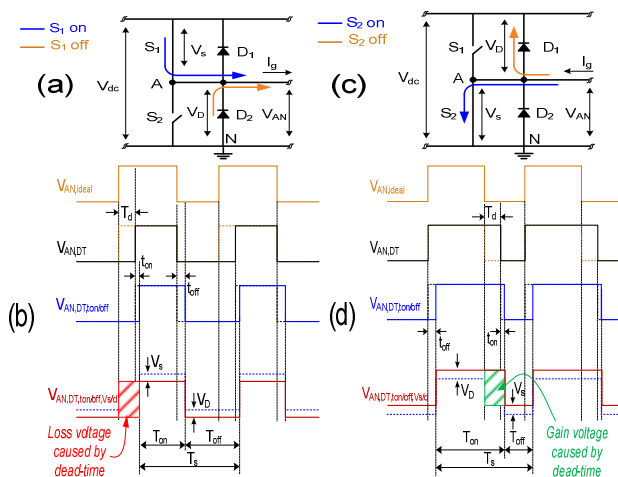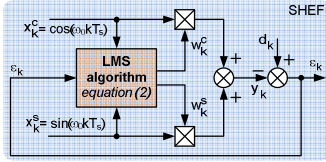
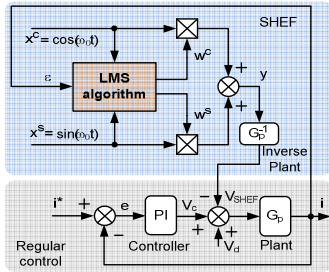Fig. 2. Single-frequency selective harmonic elimination filter

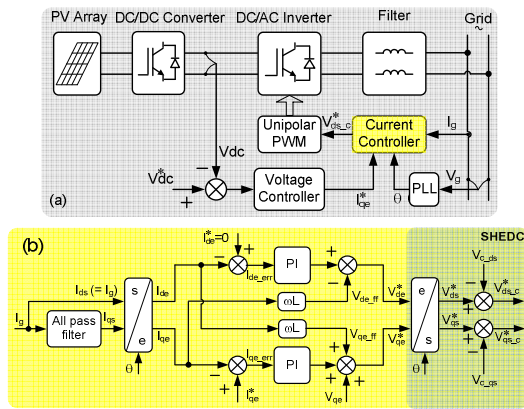Fig. 3. Integration of SHEF and regular plant control part

Fig. 4. (a) Current-controlled based single-phase PV system and (b) detailed current controller with SHEDC integration
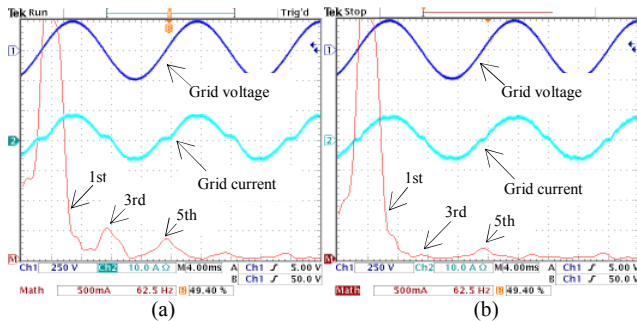

Fig. 5. Grid voltage, grid current and its frequency spectrum (a) without dead-time compensation and (b) with dead-time compensation

Some assumptions are made to ensure no interaction between the regular control and the filter:

- The adaptation process of the filter is slow. Therefore, the filter does not interfere with dynamics and does not alter the transfer function of the plant and associated control.
- The harmonic component frequency to be eliminated by the filter is higher than the bandwidth of regular control.
- The harmonic in current changes slowly to allow SHEF adjusts the weight functions and eliminates the higher harmonic components.

A simplified block diagram of SHEF and regular plant control integration in synchronous frame is shown in Fig. 3. Because of the same structure, the subscript d and q are omitted. The objective is to eliminate undesired harmonic component from plant output

which is created by the distorted voltage V_d. The elimination is accomplished when output voltage of SHEF (V_{SHEF}) matches with V_d in the signal.

The block diagram of single-phase PV inverter system is shown in Fig. 4(a). A SHEDC using aforementioned SHEF is applied to suppress the high frequency components from feedback current. The proposed current controller is shown in Fig. 4(b) where the elimination was done in the stationary rather than the synchronous reference frame to avoid the coupling problem in synchronous reference frame.

3. Experimental Results

A 3kW single-phase grid-connected PV inverter control system is implemented fully in software adopting a 32-bit fixed-point DSP TMS320F2812. The current controller and dead-time compensator for the inverter are implemented in software, and the PWM pulses are generated through the internal pulse generator of the DSP.

Fig. 5(a) shows the grid voltage in channel 1 (250V/div), grid current in channel 2 (10A/div) and its frequency spectrum in channel M (500mA/div) when no dead-time compensator is adopted. As shown, the dead-time effect causes the zero-crossing error and creates 3rd and 5th harmonic components in the grid current.

When dead-time compensator is applied, the experimental results are shown in Fig. 5(b) with the same channels and scales as in Fig. 5(a). As shown in Fig. 5(b), the dead-time effect around the zero-crossing point and 3rd and 5th harmonic components are mitigated.

4. Conclusions

In this paper, a new software-based on-line dead-time compensation technique for single-phase grid-connected PV inverter system is proposed. By using a selective harmonic elimination of instantaneous feedback current as an additional part of conventional current control loop, the effectiveness of dead-time around the zero-crossing point can be mitigated. The proposed compensation scheme does not require any external hardware or any off-line experimental measurements. Furthermore, this algorithm can be easily implemented and applied both in the transient-state and steady-state.

Reference

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